

MILLIMETER-WAVE DRIVER
AMPLIFIER: A MMIC APPROACH

by

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A Design Project submitted in fulfillment
of the requirements for

EE 801

JOHNS HOPKINS UNIVERSITY

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Abstract

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To fulfill the objectives of EE801, “Independent Study: Topics in Electrical Engineering”, a design project consisting of a MMIC millimeter-wave amplifier was selected. At the onset of this investigation, a broadband device with useable gain, noise figure and output power across 20-40 GHz was desired. Such a device would find extensive applications in the emerging LMDS (Local-Multipoint-Distribution Service) market as a driver amplifier in portions of the microwave spectrum recently made available by the FCC. Also, such a device would find use in tactical systems such as airborne radars, spacecraft communications/surveillance payloads or electronic counter-measures, where size is at a premium.

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Introduction

Circuit Description

Amplifiers find applications in most any type of microwave receiving or transmitting system. The process of signal amplification is basic to the task of signal detection or transmission. With the recent availability of millimeter-wave spectrum, commercial providers of broad-band services are in need of low-cost, highly integrated devices for use in next generation cellular products and information appliances. At the present time, there is dearth of broad-band gain blocks covering the 20-40 GHz band. Moreover, much of the presently available devices are large, discrete-based designs rather than smaller MMICs. As fabrication techniques have matured, the possibility of millimeter-wave MMIC amplifiers has become feasible. For this design, P-HEMT devices realized in Gallium Arsenide are utilized as the gain elements. P-HEMT devices, by the nature of their pseudomorphic junctions, tend to operate at very high frequencies and exhibit exceptionally low noise figure.

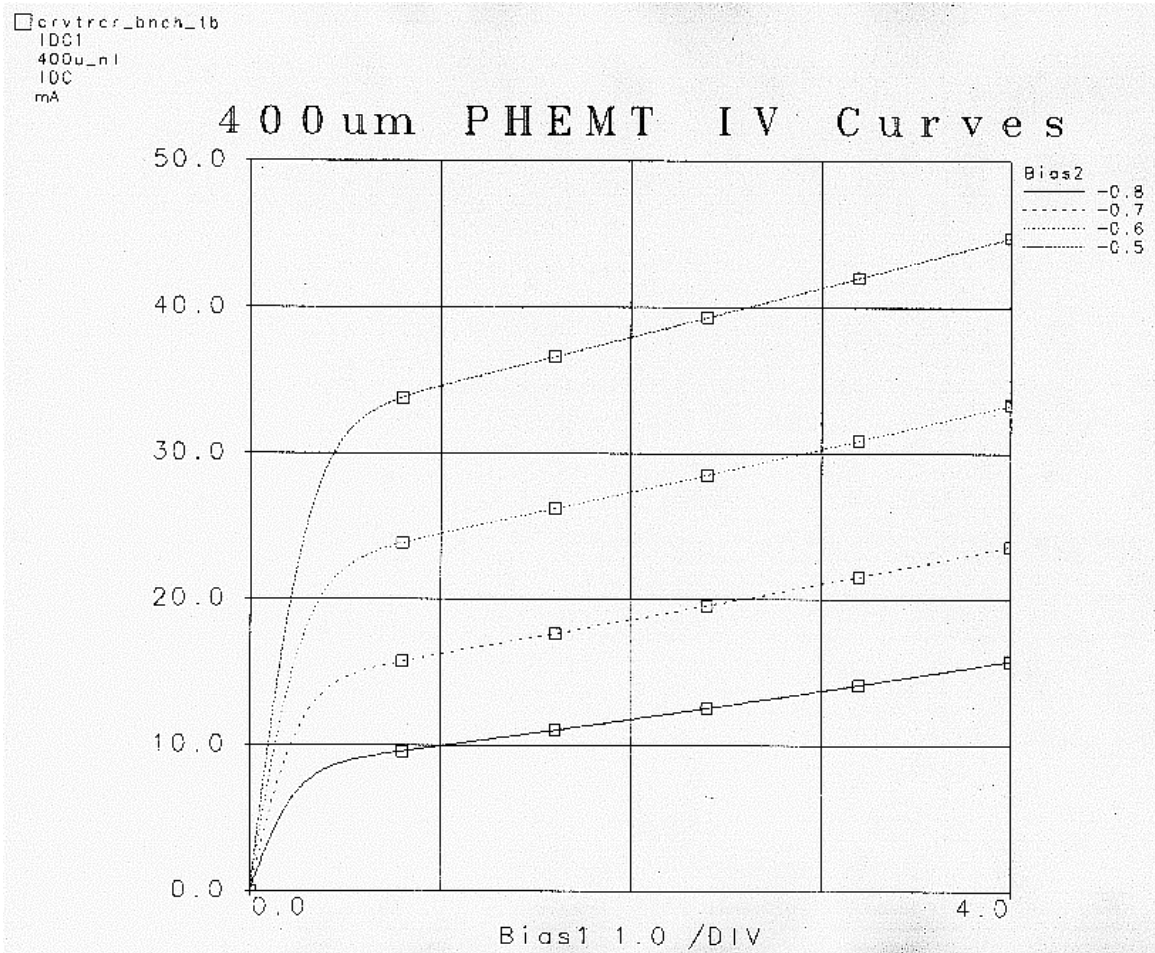
A balanced amplifier architecture was used for this design. Early in the investigation, it was found that a single FET amplifier would not exhibit much useable gain over an octave band, much less a sub-octave. The balanced configuration permits the use of more than one device and provides for some phase cancellation of device mis-match. However, these come at the price of higher loss at the front end, compromising noise figure. Lange couplers are used as the combining elements, as they can be reasonably realized in monolithic form at 30 GHz. The balanced amplifier consists of two stages, each using 8x50 um P-HEMTS power-combined, for a total of four transistors. A linear model fit to swept data was provided by the device manufacturer. A proprietary non-linear Materka model based on extracted device parameters was also provided to

generate IV curves, output power, third and second order intercept and power-added efficiency simulations. Each device is biased identically, though provision is made in the design to independently adjust the biases during laboratory tests. The drain bias lines of each device also serve as part of the output matching network. The output match consists of a high-impedance open stub and a low impedance series-connected transmission line. The input matching network consists of shunt capacitor and low-impedance transmission line. Gate bias-tees are realized as conventional quarter-wave structures with large bypass capacitors. At these high frequencies, distributed matching techniques do not consume as much circuit real estate, moreover, the utility of purely lumped element matching techniques becomes minimal beyond 20 GHz.

Design Philosophy

At the onset, several possible device architectures were explored. A feedback amplifier and a two-stage design were analyzed. The feedback design exhibited minimal gain and poor noise figure. Also, it was not readily apparent how to realize the series inductor-capacitor-resistor (at these frequencies) required to couple signal energy from output to input. This approach was quickly abandoned for the simpler two-stage design. Unfortunately, this design was unable to achieve broad-band performance. Both designs were made to be unconditionally stable from 1 GHz to beyond 40 GHz using a parallel resistor-capacitor combination at the device input. MU and K parameters were both simulated. A low value shunt capacitor at the transistor gate was found to make the input matching network design far more tractable and aided in stability. Both designs made use of “noise circle” and “gain circle” design techniques. The input matching networks were designed to present the transistor gates with the optimum reflection coefficient for low-noise operation. Due to the stability of the devices, a simple conjugate match was used as the basis of the output matching network design.

Of the two designs, the two-stage design yielded the most promise. In order to broad-band the gain, a “high-low” design approach was pursued. Noise circles and conjugate matching techniques tend to work well over narrow-bandwidths. At bandwidths approaching an octave, variation in the input and output impedance of most solid-state devices makes this design methodology more difficult to apply. However, the use of two stages permits some flexibility. The “high-low” approach involved designing and tuning the first stage at a low frequency (the low end of the band), using the familiar noise circle/conjugate matching techniques. The same procedure is applied to the second stage, only for the higher end of the band. Both stages are then cascaded, yielding a double-tuned response. However, both devices are matched well to 50Ω over only a subset of the desired band. The trick is to have the second stage response to complement the first stage response to provide gain equalization. Inter-stage Matching networks are then tuned to “de-Q” the double-tuned response and achieve gain flatness across the band. One of the target goals for this design was a noise figure 3 dB or less, with a linear gain greater than 10 dB. Also, a saturated output power of approximately 15-20 dBm was desired. These initial specifications provided the basis for bias point selection. Data provided by the manufacturer and simulation of designs based on slightly different bias points quickly narrowed down the possibilities. In order to best meet the aforementioned specifications, a gate bias of -0.6 V with the drain at 3 V was selected. Measured data from the manufacturer indicated this would yield a drain current of $\sim 20 \text{ mA}$, which was low enough to keep the noise figure from growing too large, yet high enough to anticipate a reasonable amount of output power. Noise figure is a strong function of device bias. High levels of current are indicative of many charge carriers. The more carriers, the larger the noise process and subsequent increase in device noise figure. Simulations carried out with the provided Materka models yielded a slightly higher current than the manufacturer’s data indicated. The models were initially for a 600um device, however the area

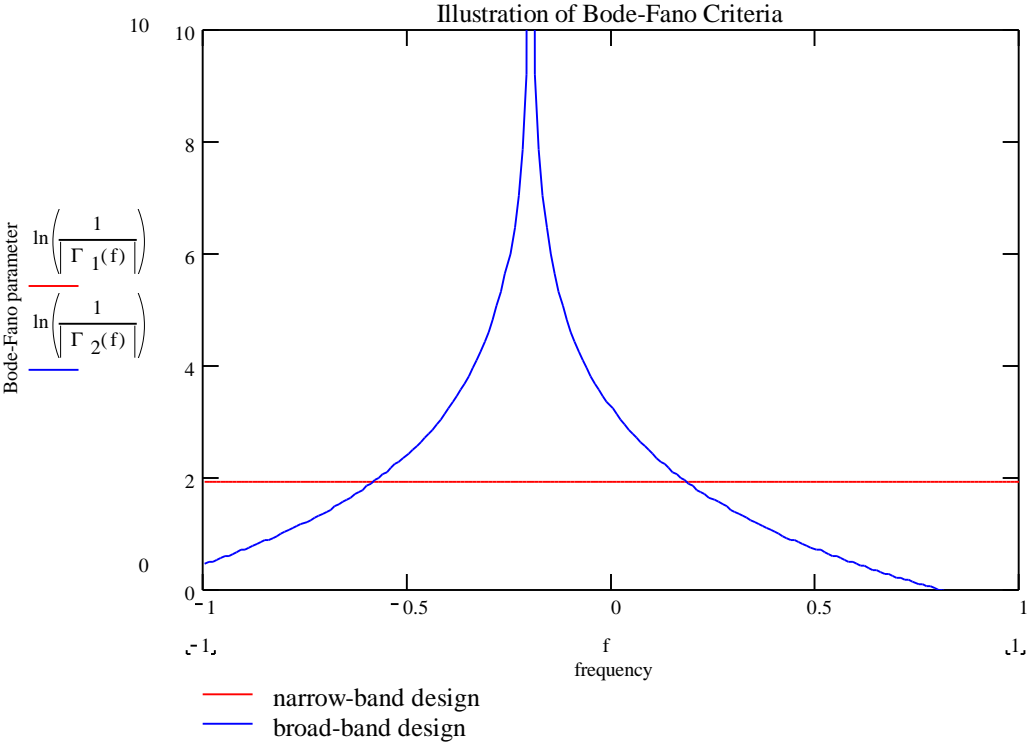


parameter was scaled to represent a 400um transistor. The final design will have provision for independent bias adjustments, so this discrepancy can be addressed during device measurement and test.

Trade-Offs

Early in the design, compromises had to be made. It became apparent that achieving a full octave bandwidth (20-40 GHz) was going to be very difficult with the chosen two-stage design. Another architecture, such as a distributed amplifier may have been explored to achieve the desired full octave performance, but distributed amplifier designs tend to have other undesirable characteristics such as low gain and high noise figure. Judicious tuning and adjustment of inter-stage matching networks ultimately yielded a design exhibiting 13 dB gain (± 1 dB) from

25 to 33 GHz. The 3 dB bandwidth of the device extends from 24 to 34 GHz. Noise figure is less than 4 dB across this band. In effect, noise figure and gain were traded-off for improved broad-band performance. The well known Bode-Fano criteria supports this observation, whereas there is a limit to the extent at which a matching network can be improved. In essence, a nearly “perfect” match can be obtained at a single frequency, however, examination of the Bode-Fano parameter shows that this may not be the most efficient way of achieving a broad-band match. By trading off reflection coefficient magnitude over bandwidth, a better match may be achieved over a broader band, yet it will be less than the “nearly” perfect match over a narrow-band. The areas bounded by the two integrals are equal, yet in the case of the broad-band amplifier, the input reflection coefficient is higher.



Another target goal for the design was creating a device which would fit in a 60x100mil chip area. As the design progressed, the two-stage design morphed into a balanced configuration using two Lange couplers. Each “stage” then became the double-tuned, “high-low”, two-stage design. A six-section Lange gave better broad-band performance, yet introduced excessive insertion loss which compromised noise figure. In the end, a four-section Lange coupler centered at 30 GHz yielded satisfactory performance. The progression to a balanced design quickly consumed the available real estate. Instead of two 400um devices, the design now had four, with four biasing networks instead of two. However, since the performance of the amplifier dramatically improved, it was agreed to allow the design to grow. In its final rendition, the design will most likely be fabricated on a 120x150mil size chip.

Modeled Performance

Specifications

The following target specifications were used in design of the MMIC amplifier. Simulated performance numbers are also listed.

<u>MMIC AMPLIFIER SPECIFICATION MATRIX</u>		
Frequency: 20-40 GHz		
Desired Size: 60x60 mil		
<u>PARAMETER</u>	<u>TARGET GOAL</u>	<u>POST-LAYOUT SIMULATION</u>
GAIN	15 dB (10 dB min)	*24-34 GHz 3 dB BW 11 dB at band edges 14 dB at 30 GHz
NOISE FIGURE	2 dB (3 dB max)	*24-34 GHz 4 dB
RETURN LOSS (INPUT/OUTPUT)	15 dB (10 dB min)	*25-36 GHz >10 dB
SATURATED OUTPUT POWER	20 dBm (15 dBm min)	*24-34 GHz 20 dBm

Additional parameters not specified, but also simulated, are included for reference.

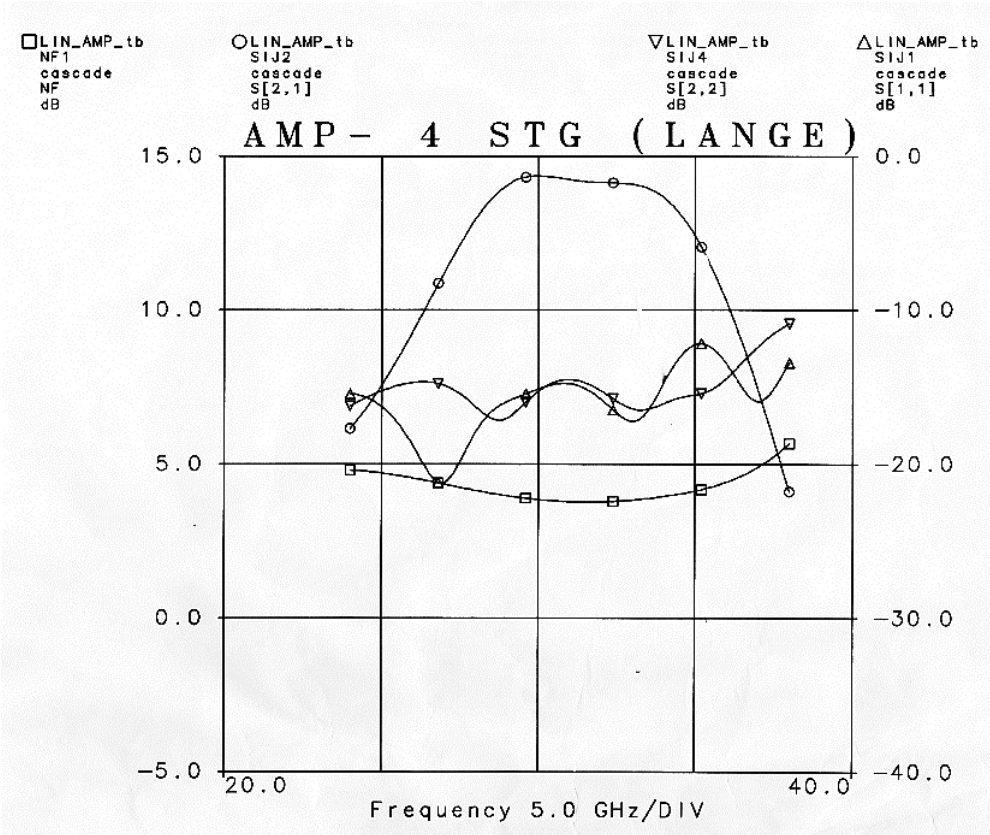
<u>ADDITIONAL SIMULATED PARAMETERS</u>	
<u>PARAMETER</u>	<u>POST-LAYOUT SIMULATION</u>
Third-Order Intercept Point	
Second-Order Intercept Point	
Power-Added Efficiency	18.6%

Predicted Performance

As has been already stated, several different implementations were explored. Each approach had its merits, yet an optimal solution to all initial specifications proved difficult. A balanced amplifier design proved to yield the best performance compromise. Linear S-parameter simulations were conducted using a linear model fit to measured device data. Harmonic balance non-linear simulations using a scaled version of the 600um Materka model were also performed.

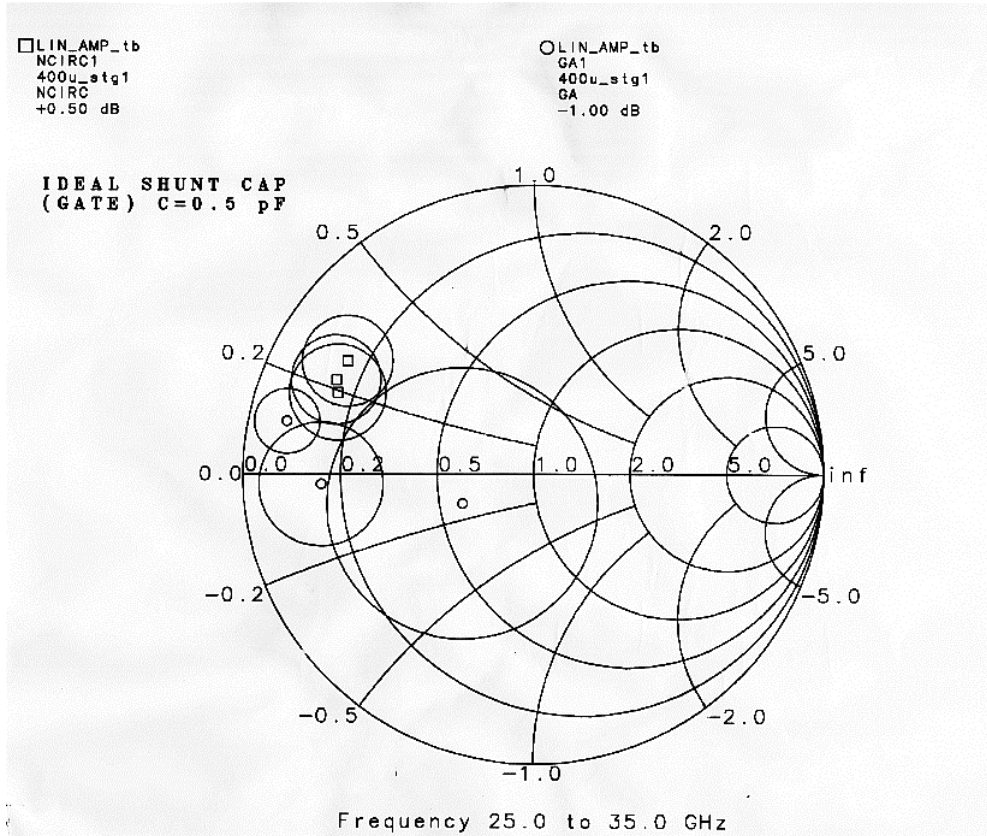
Prior to layout, the design was optimized using ideal elements. Performance of this virtual “proto-type” was satisfactory. In particular, the bandwidth was narrower than the design goal and the noise figure was slightly higher. Return loss was within specification. At these frequencies of operation, there is some uncertainty as to the accuracy of the Series IV models for transmission lines and interconnects between components. Parasitics have a much more pronounced effect on circuit performance as frequency increases. In particular, a low-value

shunt capacitor was used at the transistor gate to move the noise-match points closer to the real axis. Doing this allowed a $50\ \Omega$ match to be obtained by simply using a length of low-impedance transmission line. This suggestion was provided by Craig Moore to John Penn. However, there was concern that the low value capacitance would be shifted in value due to the metal interconnects introducing

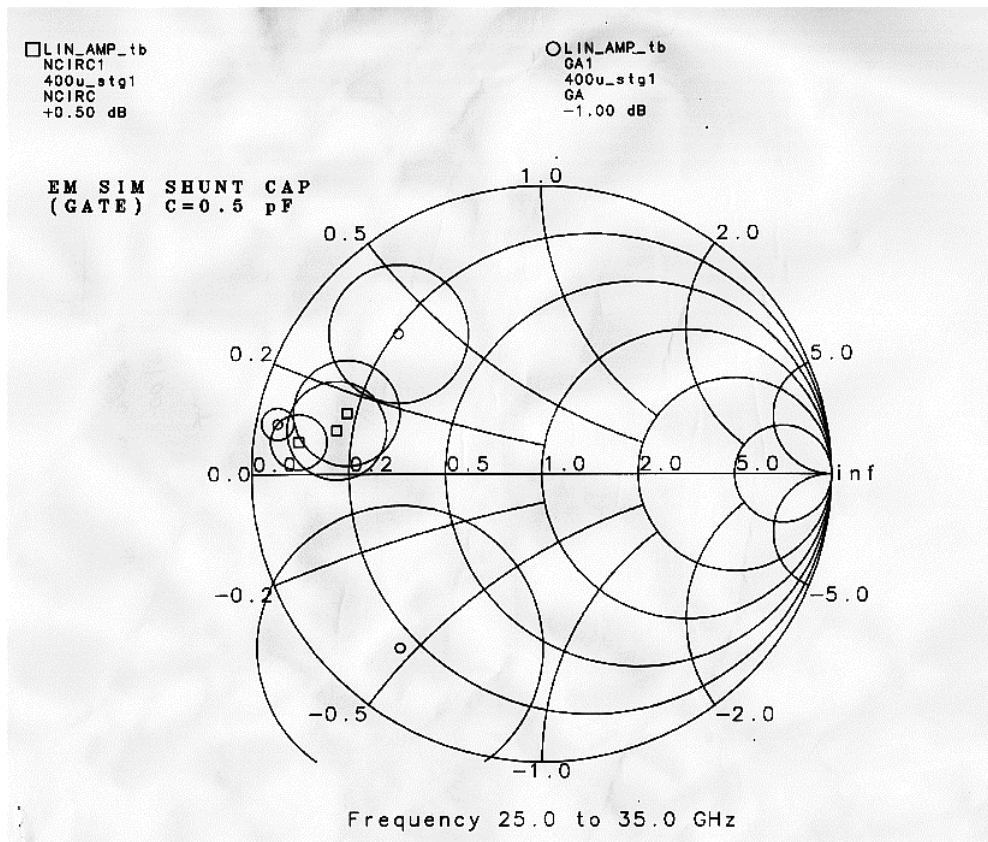


additional reactances at these high frequencies.

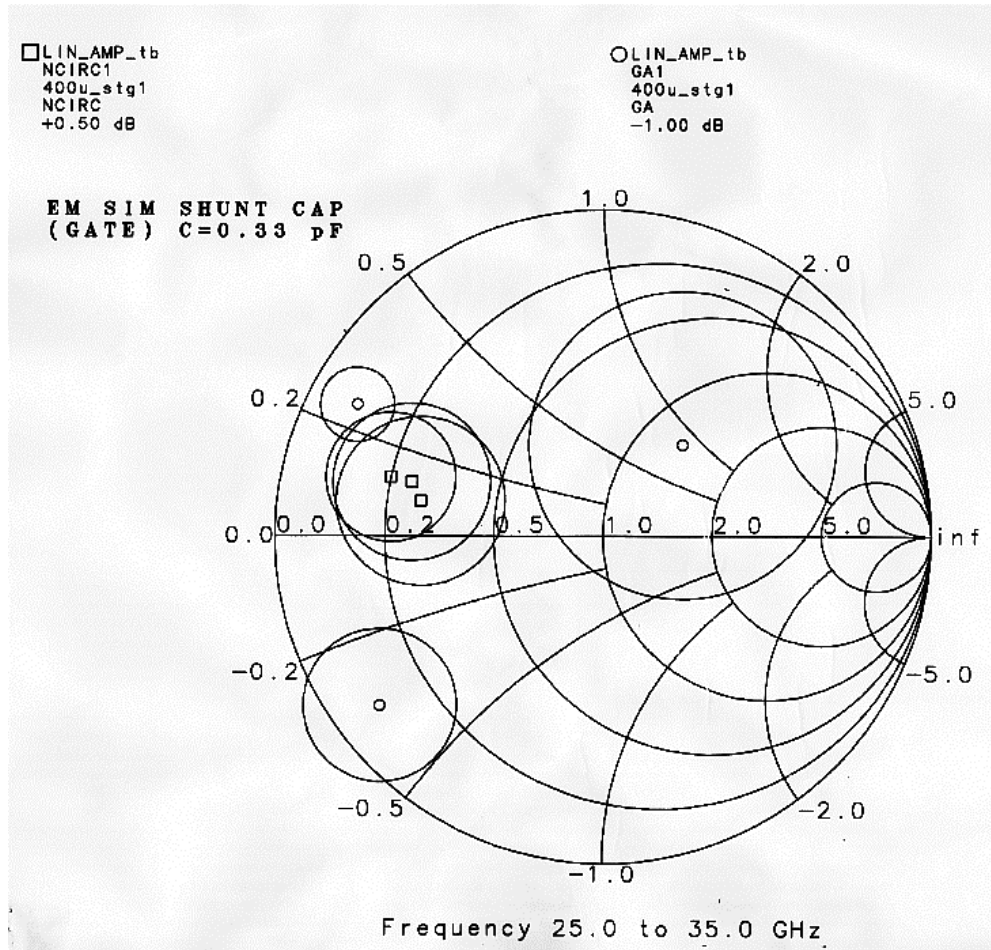
In order to perform a sanity check on the simulations, John Penn provided S-parameter data of a physics-based full-electromagnetic simulation of the planar capacitor structure, for 0.33 and 0.5 pF capacitors. The ideal capacitors were removed from the simulation with the two-port data from the EM simulation as substitute. The ideal simulation predicted a shunt capacitance of 0.5 pF.



The simulation using the EM-physics based data is markedly different from the ideal circuit simulation. It appears that the 0.5 pF capacitor is a bit too high in value. The primary impact on the amplifier performance was the introduction of a severe low-pass response which down-shifted the high-end frequency response by roughly 5 GHz. Another simulation using a 0.33-pF capacitor (EM data) shows better agreement



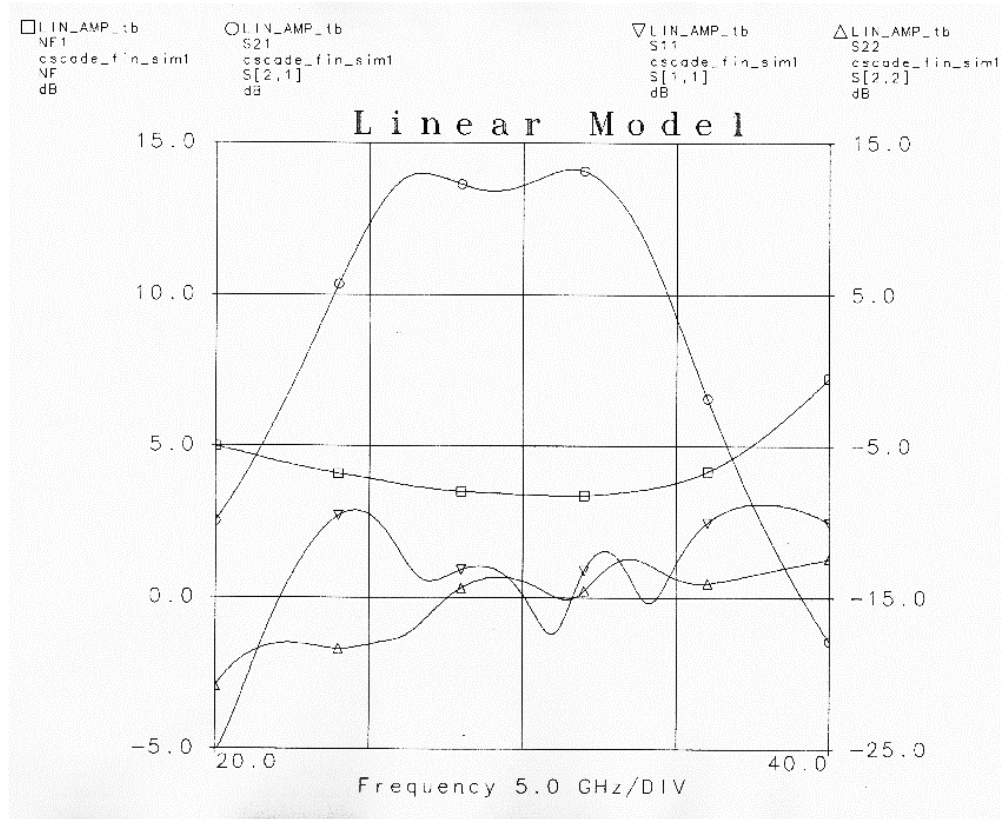
The 0.33-pF capacitor was ultimately used in the design. Provisions were made in the capacitor implementation to allow for a modest level of tuning. A “tuneable” capacitor using conductive epoxy to adjust capacitor cells was envisioned.



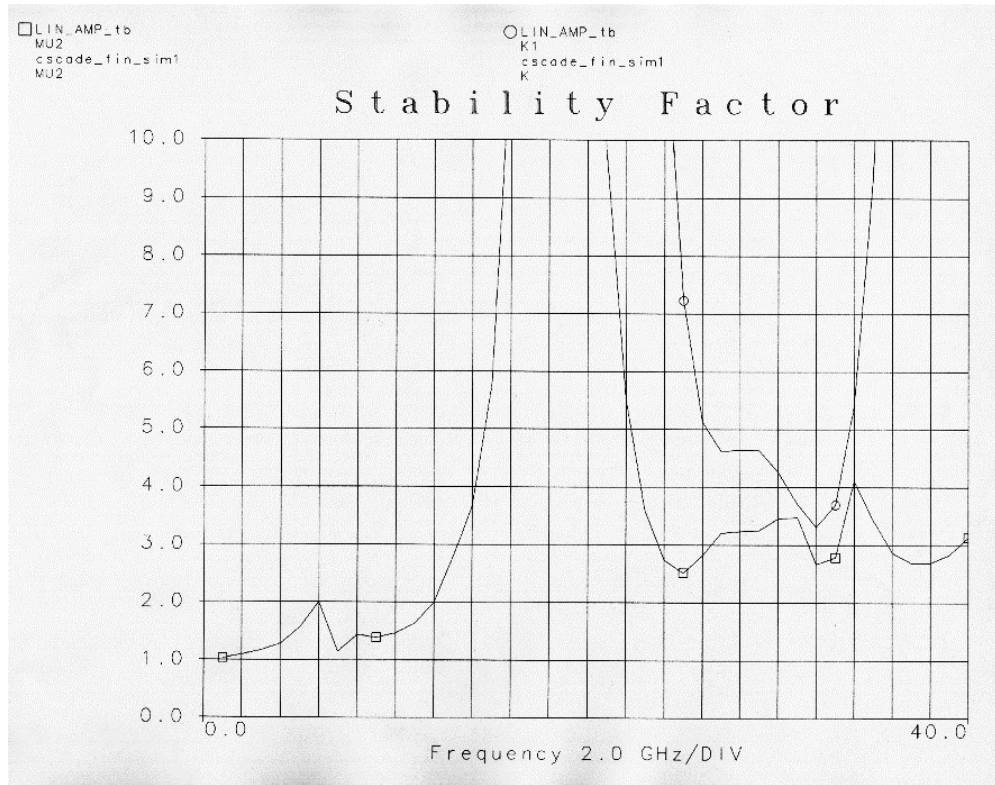
This will allow some amount of post-production tuning, should there be any shift in the actual capacitance.

With the input capacitor issue resolved, the design tasks focused on the tuning of inter-stage matching networks to recover bandwidth. Gain was simulated using the linear model and the non-linear Materka model under small-signal conditions. The first iteration of the balanced amplifier utilized a drain biasing network separate from the output matching network. An attempt was made to combine the drain bias and output matching network to save chip real estate. The final revision of the design utilized the drain bias lines to provide the shunt inductor

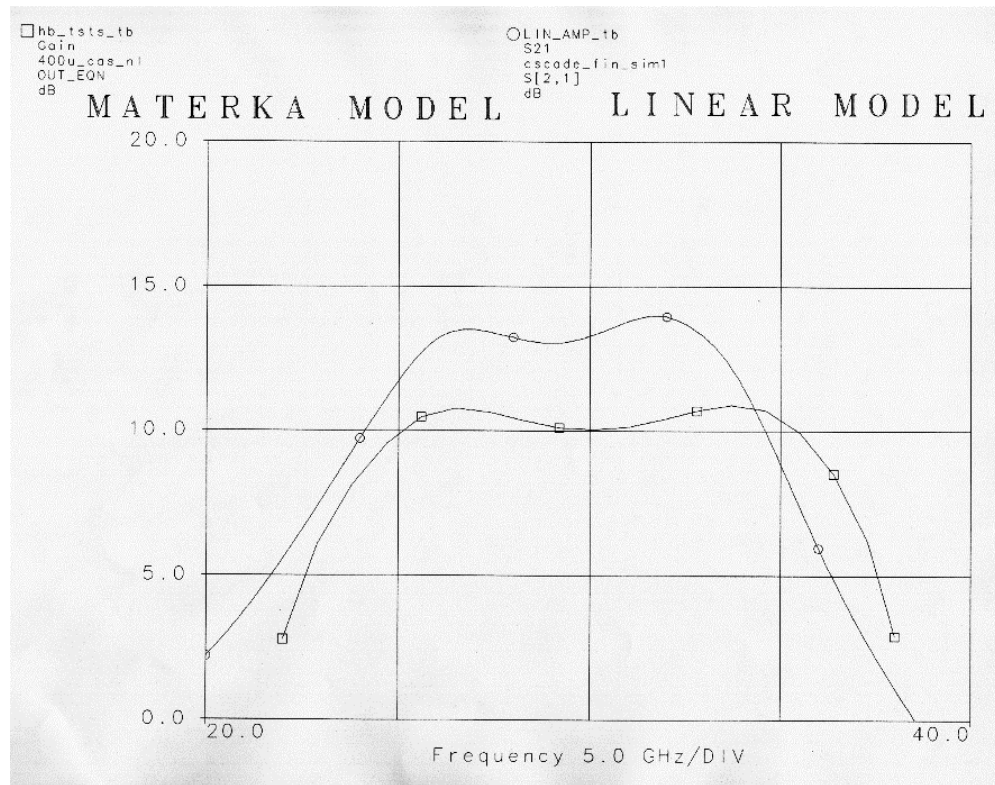
required in the output matching network. Only minor tuning was required to recover the device performance.



Gain and noise figure are both close to the original design specifications, though there is little margin.

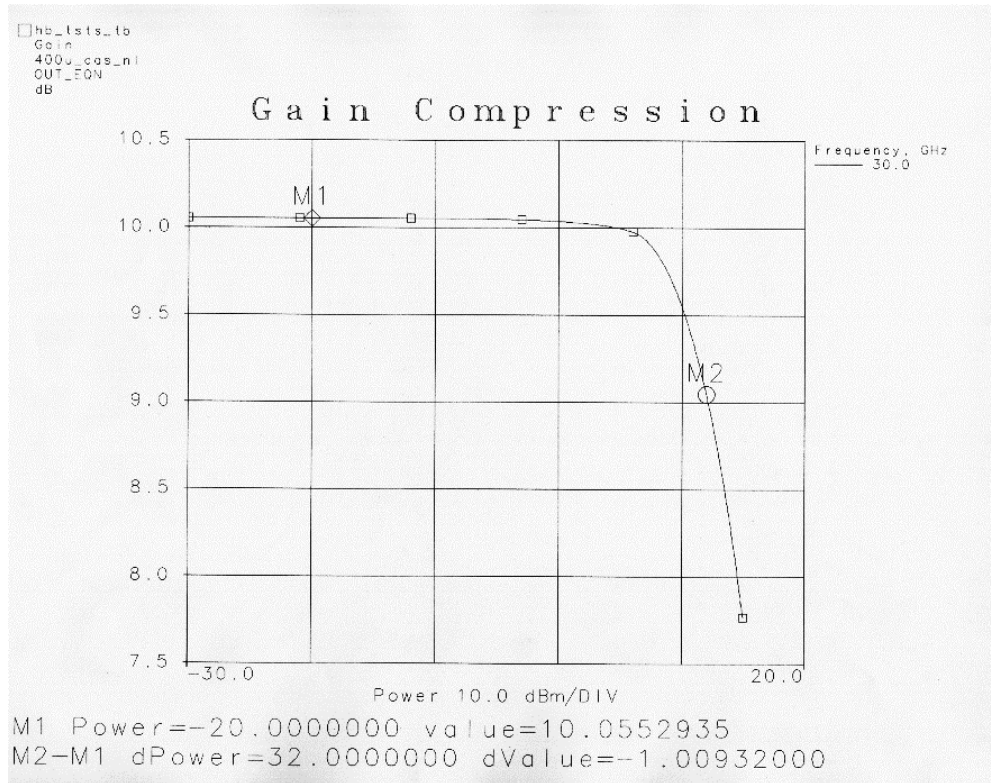


Stability was also checked for each stage and the completed amplifier. The design is unconditionally stable from 1-40 GHz.

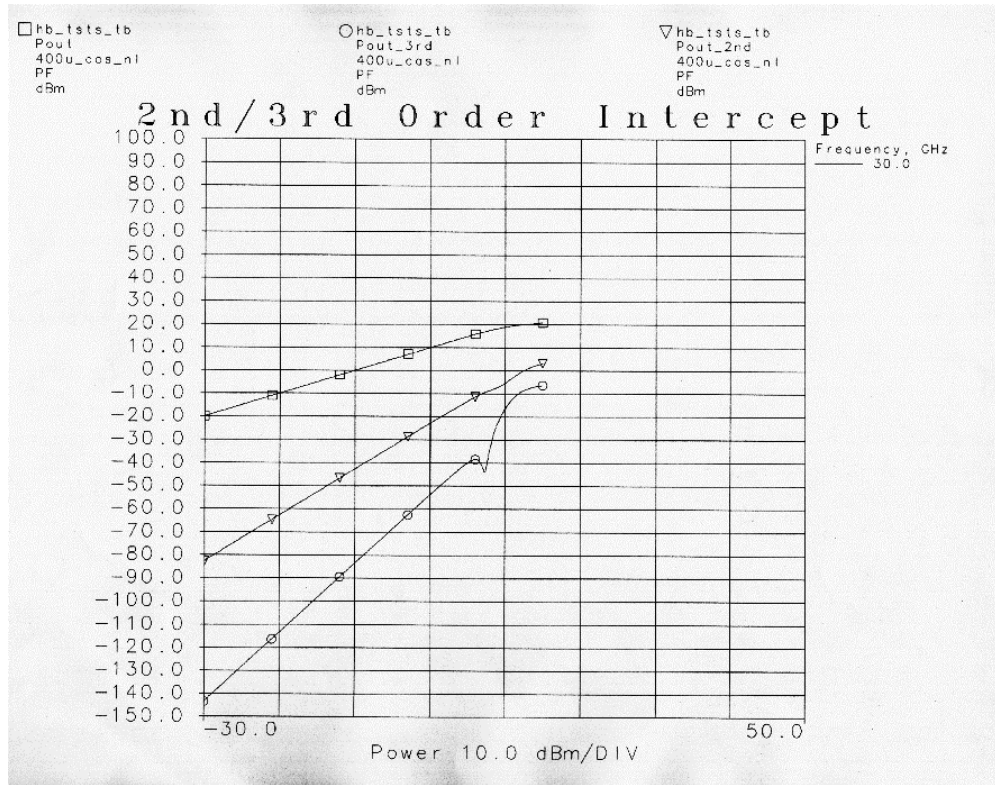


A “manual” equation for gain was written in the Series IV harmonic-balance test bench to simulate small-signal gain using the Materka model. Input power was set to -20 dBm to ensure small signal conditions. The basic form of the gain response agree between the two simulations, however the Materka model predicts 3-4 dB less gain.

One-dB compression point was also simulated using the non-linear model and harmonic balance test bench. The one-dB compression point is $+12$ dBm, with 9 dB of gain, for an output power of $+21$ dBm at 1 dB gain compression. These numbers exceed the original specifications.



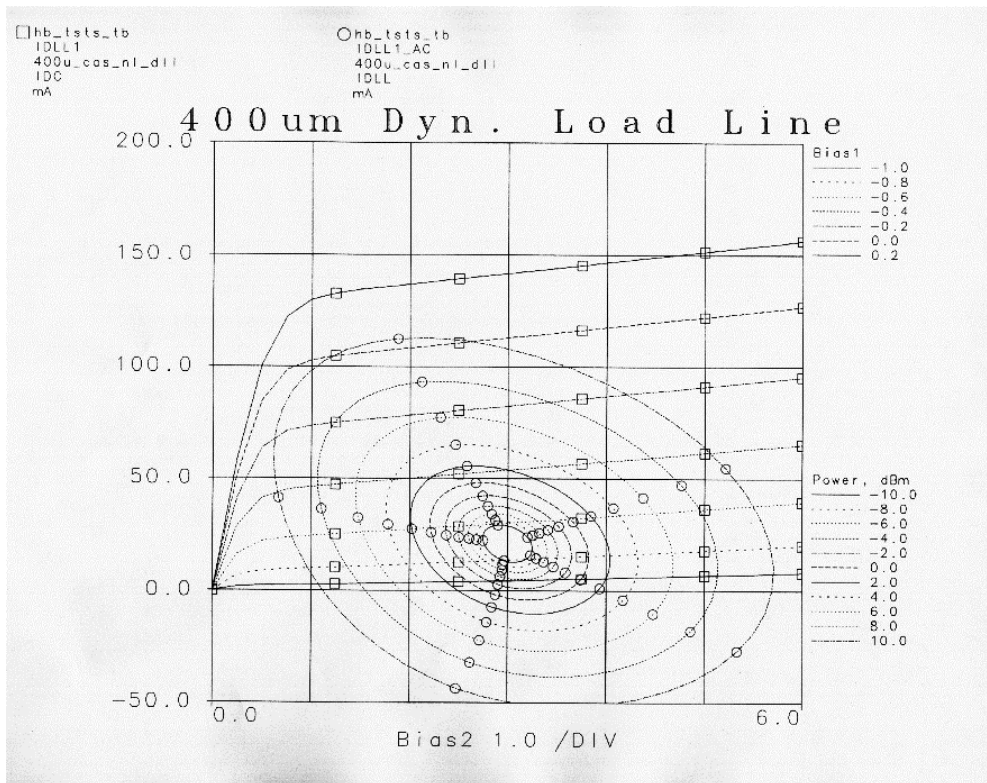
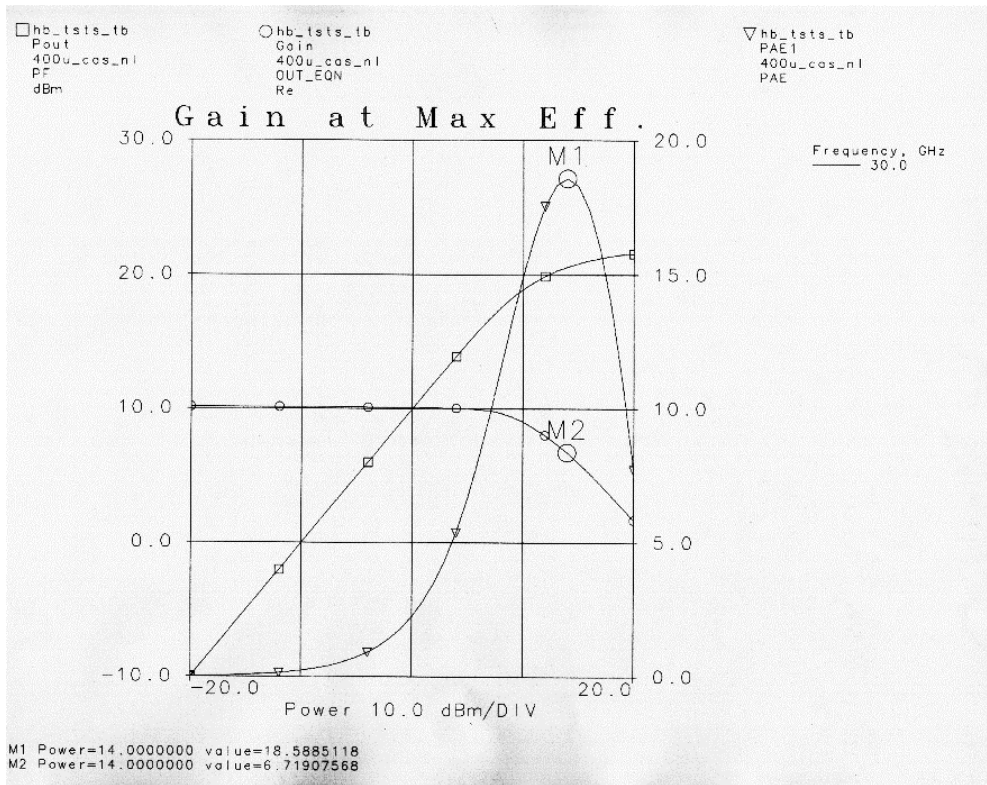
Additional parameters were also simulated to fully characterize the amplifier. Plots are included of: 1. 2nd/3rd order gain slopes (to calculate 2nd and third order intercept points), 2. PAE (power-added efficiency, and 3. Dynamic Drain Current Load Line (single transistor, part of output stage).



Extrapolation of the third and second order slopes yield a second order output intercept point of + dBm and a third order output intercept point of + dBm, respectively.

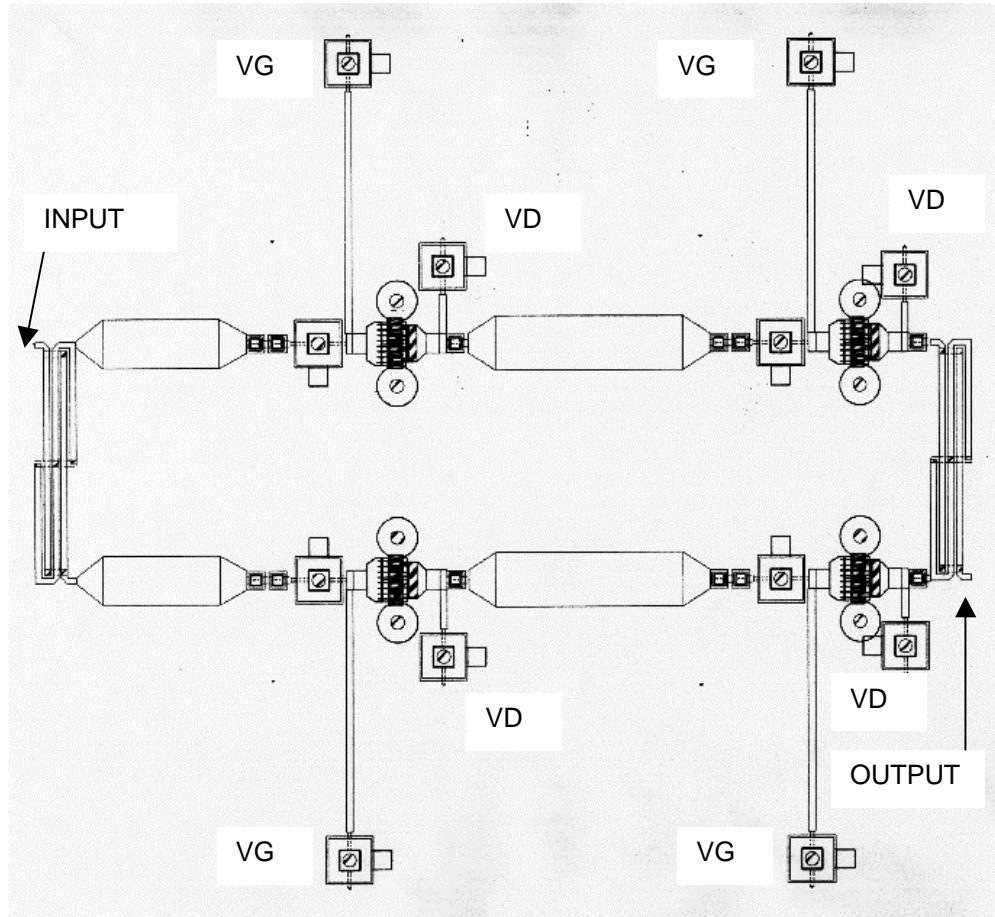
Probed Response

TO BE ADDED AFTER CHIPS ARE MEASURED IN WINTER OF 2001.

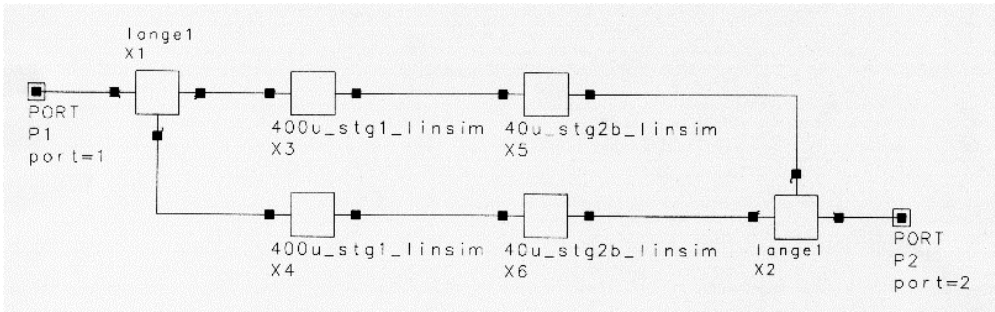
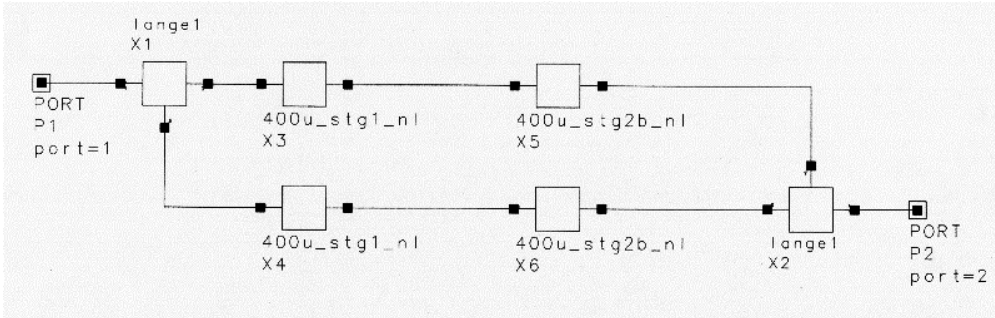


Schematics

Final Layout



Final Electrical Schematic



*Schematics for each individual sub-circuit are attached separately for brevity

DC Schematic

DC Analysis

Component Current Stress

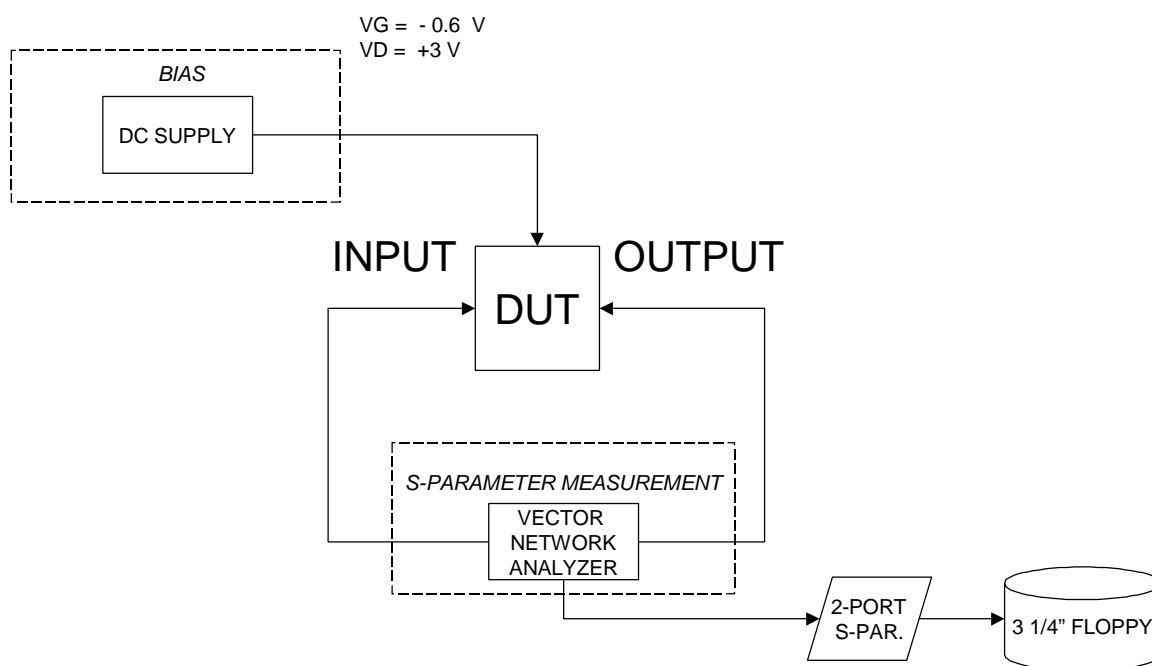
One of the chief causes of device failure in MMICs is mis-applied DC bias, or incorrectly designed bias networks.. Oversight in the design of the bias network can lead to currents that may exceed the handling capability of metal interconnect traces or the rating of bias resistors. Thin, purposefully inductive bias lines may not be able to carry the required DC current. Currents in specific bias branches, trace width, and device technology were analyzed to determine if any bias currents exceeded the ratings of the MMIC structure.

<u>DC BIAS CHECK</u>			
BIAS POINT	CURRENT/ VOLTAGE	MINIMUM LINE WIDTH	RESISTOR SIZE/TYPE
GATE –INPUT & OUTPUT STAGES	minimal current/ -0.6 V	10 μm	N/A
DRAIN – INPUT & OUTPUT STAGES	20 mA/ 3V	25 μm	N/A

10 μm wide line (interconnect) can handle up to 180 mA. Currents are well within the capabilities of chosen device technology.

Equipment Diagram

TEST SETUP - S-PARAMETER MEASUREMENT

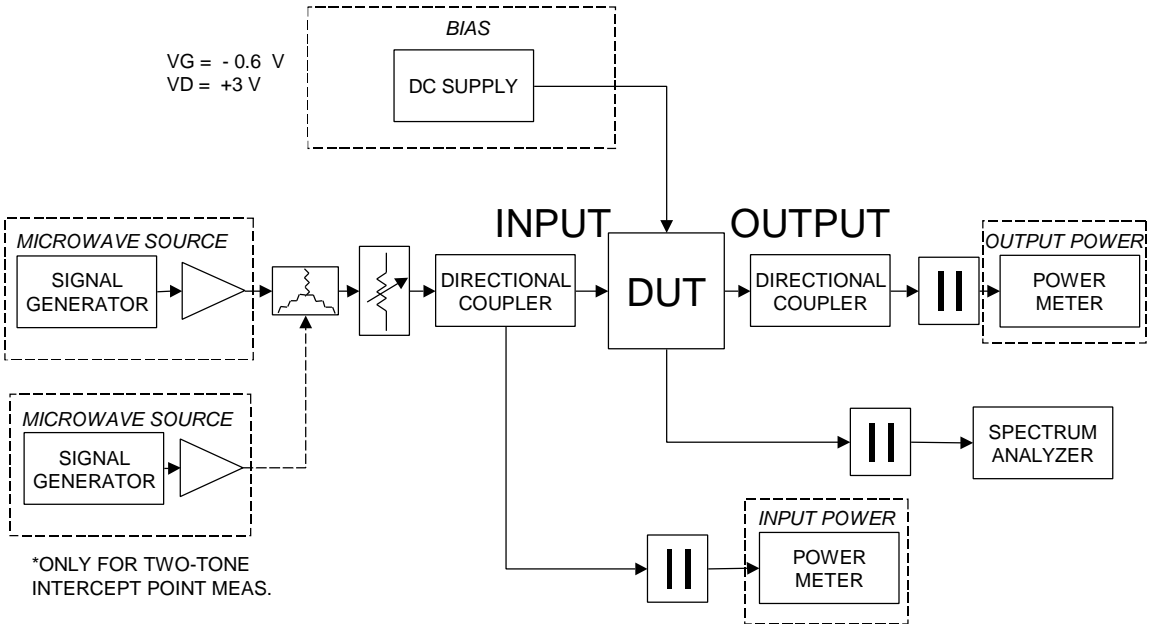


This test set will be used to obtain two-port S-parameter data for the amplifier. The data will be written to a floppy in a magnitude/phase format. Hard copy plots can be immediately generated in log-magnitude format; to get immediate results for gain, in/output return loss and isolation, however, the S-parameters on disk will allow computation of other parameters, such as stability. Since the amplifier operates roughly from 25 to 35 GHz, appropriate low-loss coaxial cables should be used for all RF interconnects. All connector interfaces should be cleaned with alcohol or another suitable solvent to remove any fine particles

that would corrupt the measured response. At these high frequencies, such special care is mandatory. Prior to making measurements, All instruments must be calibrated and cable losses accounted for.

In order to measure device output power (under large signal conditions) and third order intercept point, a different test set is required (shown below). The same general precautions should be followed when assembling and calibrating the equipment.

**TEST SETUP - LG. SIG. OUPUT POWER
INTERCEPT POINTS**



REQUIRED TEST EQUIPMENT

***ALL MICROWAVE INSTRUMENTS MUST PROVIDE 20-40 GHz COVERAGE**

INSTRUMENT/DEVICE	QUANTITY
Quad-output DC Lab supply	1
Microwave Signal Generator	2
Power Amplifier (+20 dBm Pout)	1
Microwave Spectrum Analyzer	1
Adequate supply of low-loss coaxial test cable and connectors	N/A
Wafer probe station, microwave probes, needle probes for biasing	1 station
Microwave Power Meter	2
Directional Bridge	1
Directional Coupler	2
Microwave Step Attenuator	1
Microwave Vector Analyzer or Eqv.	1

Biasing Procedure

1. Connect all test equipment per the attached test setup diagram.
2. Mount the mixer MMIC in the probe station test fixture
3. Set power supply to -0.6 V, and $+3$ V. Set the current limit to 150 mA.
4. Using needle probes, apply -0.6 V GATE voltage FIRST, then apply 3 V DRAIN bias.

S-Parameter Measurement Procedure

1. Set the network analyzer to provide -20 dBm output power; this will ensure the amplifier is operating under small signal conditions.
2. Calibrate the network analyzer for a full two-port measurement. Set the start frequency to 20GHz, the stop frequency to 40 GHz and number of sweep point to 801. Connect device as shown in first test diagram, note current draw on power supply.
3. Generate hardcopy plots of all four S-parameters using a "log-magnitude" format. Save softcopies of the S-parameters to disk using a complex "magnitude-angle" format.

Output Power Measurement Procedure

1. Do NOT hook up RF power to the DUT yet! Set the microwave source to provide a single tone at 30 GHz. The output power of the source/amplifier combination should be about $+20$ dBm.
2. Using the step attenuator and noting the coupling ration of the directional coupler, measure 0 dBm at the output of the step attenuator.

3. Connect the DUT input as shown in the diagram. Note the output spectrum and power level. Step the input power in one dB steps using the step attenuator, up to +15 dBm input power (measured in the input coupler). Note the output power and point where signal gain decreases by one dB (one dB compression point). Note current draw on power supply.

Two-Tone Third-Order Intercept Point

1. Connect all test equipment as shown in the second test diagram. Using the step attenuator and power meter, ensure the RF power does not exceed –20 dBm. Set microwave source #1 to 30.1 GHz. Set microwave source #2 to 29.9 GHz.
2. Note the noise figure and third-order intercept points of the spectrum analyzer. It may be necessary to use a buffer amplifier or adjust the spectrum analyzer resolution bandwidth. The spectrum analyzer should have an intercept point at least 20 dB higher than the DUT so that accurate measurements can be made.
3. Set the spectrum analyzer to a center frequency of 30 GHz. Two tones should be visible, plus the third-order product side-bands: (2 X input tone #1)-(tone #2) and (2 X input tone #2)-(tone #1). Set the bandwidth to 500 MHz.
4. Step the input power in 1dB steps until the side-bands are 5-10 dB above the noise floor of the spectrum analyzer. Generate a hardcopy plot that shows all four tones. If possible, use markers to note the delta from the main tones to the third-order side-bands.
5. Use the following formula to compute the third-order intercept point:

$$IP3 = \text{input signal level} + (\Delta \text{difference between desired and side-band})/2$$

<u>MMIC AMPLIFIER COMPLIANCE TEST MATRIX</u>	
PARAMETER	TEST
2-Port S-Parameters	X
1 dB Compression Point/Saturated Output Power	X
Input Two-Tone third order intercept point	X

C o n c l u s i o n s

Findings

A millimeter-wave, monolithic, balanced amplifier has been designed and simulated. At millimeter-wave frequencies, different techniques are used in the design of monolithic microwave components. Physics-based EM simulations of circuit structures (in particular, shunt-connected capacitors) proved to be an important tool in performing investigative predictions of the device performance. For example, the EM simulations have shown circuit parasitics to be a limiting factor in component sizing. As a result of these analyses, provisions will be made in the final design to “tune” critical capacitor values. Since the amplifier design was at such a high frequency, distributed techniques were used throughout the design. This differed from my previous experience designing MMICs at lower frequencies, where lumped techniques are solely used due the size limitations at lower microwave frequencies. Linear and non-linear methods were employed to simulate device performance. Amplifier-specific parameters that were simulated included small signal gain, return loss, large signal gain, saturated output power, noise figure, stability, power-added efficiency and second/third order intercept points. Experience was gained designing MMICs using a pHEMT process. It is hoped the experience gained will benefit other students hoping to use the pHEMT proces in future courses..

Early in the design, a feedback and simple two-stage design were explored. Unfortunately, both designs failed in satisfactorily meeting the original device specifications. Late in the design process, a balanced configuration was pursued. This design came closest in meeting the original specifications. Biasing of the amplifier was kept very simple, with gate and drain bias being applied directly. Techniques such as self biasing were not pursued, as experience with the pHEMT process was limited. Direct biasing of the gates and drains will allow

more flexibility during device test. Overall, this has proven to be a very interesting project. New design techniques for use in designing millimeter-wave monolithic microwave components were used. I gained very valuable experience and insights into the challenges of designing monolithic components at millimeter-wave frequencies.

Recommendations

In future iterations of this design, it would prove interesting to expend more effort in completely EM simulating the entire circuit structure. For this design, due to limited time, only critical components of the amplifier were EM simulated. Each key sub-circuit could be simulated using a physics-based EM simulator, such as SONNET, Agilent Technology's MOMENTUM, or HFSS. Unfortunately, these simulations can take excessive amounts of time and require fast workstations. The disparities between the ideal circuit models and the EM simulations at millimeter-wave frequencies should tend to drive designers to use more EM simulations as they pursue designs at higher frequencies.

Another area that demands some attention is the phenomena of "odd-mode" circuit oscillations. As was learned in EE788, K and MU factor analysis that is based on linear device parameters (Z or S-parameters) fails to reveal this condition. It is most often a problem in design using two or more active devices in a combiner arrangement (such as this balanced amplifier). Direct computation of the circuit eigenvalues as mentioned in Freitag's 1992 MTT conference paper is possible, however, a simpler approach using time-domain simulation has been put forward by Dale Dawson (EE788 class notes). Unfortunately, a transient simulator was not available at the time of this project to pursue this further.

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