A C-Band Power Amplifier for HiperLAN Wireless Applications

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ABSTRACT — **A 2-Stage C-Band MMIC Class-AB power amplifier (PA) was designed as part of a receiver array for the HiperLAN wireless local area network (WLAN) and industrial, scientific and industrial (ISM) frequencies. The designed was implemented for the TriQuint Oregon TQTRx 0.5-um MESFET process. Good performance in the frequency band of 5.15 to 5.875 GHz (BW = 800.0 MHz) was achieved. The PA had small-signal gain >22.0 dB across the band with an output power > +24.0 dBm and PAE of >30% at the 1dB compression point, for center frequency (f_c) 5.5125 GHz. The input, interstage and output matching networks were designed for a 50.0 Ohm system. VSWR of 1.2 and 2.1 was achieved for the input and output, respectively.**

Index Terms **— Power amplifier, Class AB, WLAN, MMIC, Efficiency, 2-stage, C band.**

I. INTRODUCTION

The initial goal was a class F design. However, with the chip size restriction of 60 x 60mil and the marginal improvement in efficiency of the class F design using these device sizes at the design frequency, it was decided that the class AB design was a better choice to meet all the design goals. The overall design goals are listed in table 1.

TABLE 1
SUMMARY OF DESIGN SPECIFICATIONS

Frequency	5150 MHz to 5875 MHz
Bandwidth	>800 MHz
Gain	>13 dB
Gain Ripple	+/- 0.5 dBmax
Output Power	>+20 dBm @ 1dB Compression
Efficiency	>20% @1dB Compression; goal = 25%
VSWR	<1.5:1 (input, output)
Supply Voltage	+/- 5 volts
Size	60 x 60 mil

The power amplifier is a 2-stage cascaded design with a pre-amplifier stage designed around a 6x50um FET and a driver stage designed around an 8x75um FET. The 300um FET in the pre-amplifier and the 600um FET were both biased for class AB operation. The 2-stage design was employed since a single stage was unable to meet the gain and power specification at the design frequency.

II. PA CIRCUIT DESCRIPTION

In consideration that this amplifier will be fabricated as a MMIC and that the layout of the amplifier is challenging, the amplifier was broken up into the sub-circuit topology shown in figure 1.

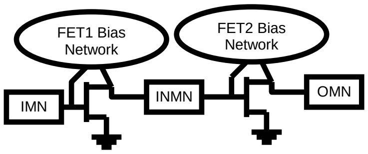

FIGURE 1: 2-Stage Amplifier Topology

This approach simplifies the layout and design optimization process tremendously. In figure 1 FET1 represents the 300um FET and FEt2 represents the 600um FET. The biasing networks utilized individual bias supply for the gate and drain of each FET.

III. DESIGN PHILOSOPHY

The design of each sub-circuit component of the PA was first done using ideal lumped elements. Those ideal elements were replaced using the corresponding models from the TQTRx design kit. Resistors and capacitors were easy to synthesize, but inductors had to be carefully modeled using an iterative tuning process. Connection of these foundry components were accomplished using microstrip lines and junctions available in the simulator (Microwave Office ™).

A. Device Selection

A 300um GFET was chosen for the pre-amplifier stage to provide high gain and good power amplification.

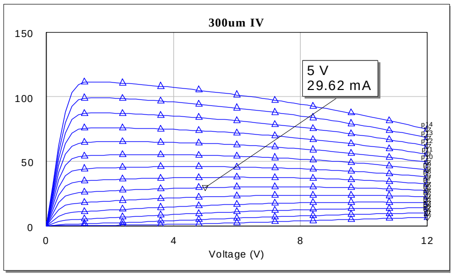

FIGURE 2: 300um GFET Operating Point

The operating point is shown in figure 2.

A 600um GFET was used for the second stage to efficiently boost the power of the pre-amp stage. Figure 3 shows the operating point for the 600um FET.

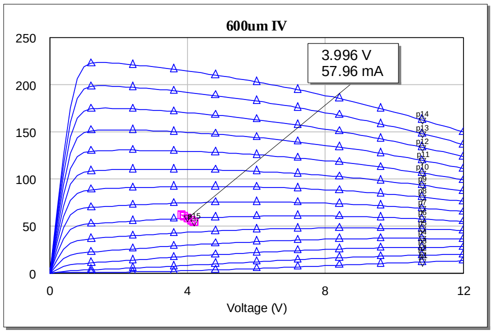

FIGURE 3: 600um GFET Operating Point

It is noteworthy that the bias points for the FETs were chosen to balance gain, power and efficiency. Another subtle goal was to allow for bias tuning. So for drain voltages between 4 volts and 5 volts should tweak the respective drain currents only slightly.

B. Biasing Networks and Stability

The biasing networks were combined with elements used to stabilize the FET. This is illustrated in figure 4.

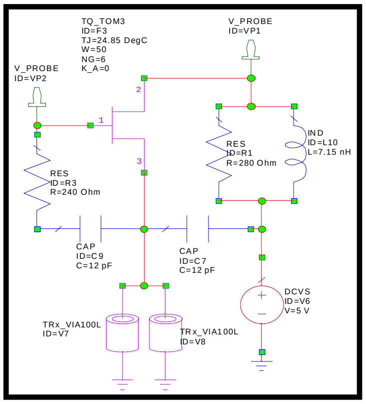

FIGURE 4: Stability/Biasing Network

The inductor on the drain side is chose to provide a convenient RF short while the shunt resistor helps to stabilize the device. The resistor on the gate side plus the small blocking capacitor on the left ensure that the supplied gate bias (shown in section C) current flows to the gate.

C. Input Matching Network (IMN)

The IMN was designed for narrow band (i.e. shortest path from generator to load). However, the path that included a shunt inductor was desired and used since this inductor can be used as the DC feed for the FET gate bias. Since it's large enough, it also provided an RF short.

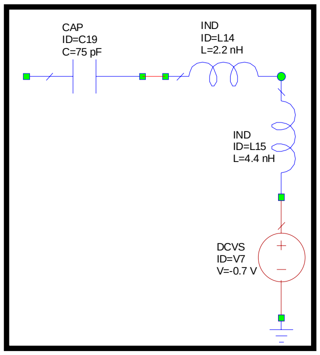

FIGURE 5: Input Matching Network (IMN)

Figure 5 shows the matching network used at the input. This was designed for a conjugate match at the input after the output matching network was designed and connected. The blocking capacitor is also included.

D. Interstage Matching Network (INMN)

The interstage match was designed as a combination of matching the output of the 300um FET and the input of the 600um FET. This technique yielded a network that was then simplified to minimize the number of elements.

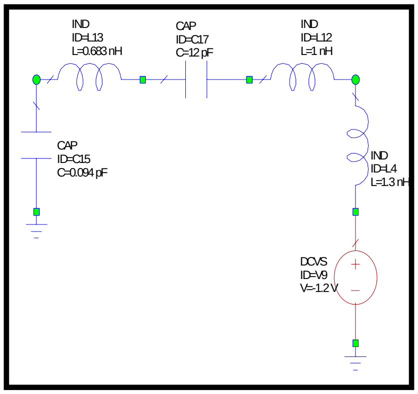

FIGURE 6: Intersatge Matching Network (INMN)

Notice (from figure 6) that the network was chosen such that the shunt inductor on the right can be used as the DC feed for the gate of FET2. A small blocking cap is inserted to direct the current from the supply to the gate of FET2.

E. Output Matching Network (OMN)

Contrary to the order in which the networks are presented in this paper the output matching network was the first to be designed. The procedure is based on the Cripps technique [1]. Rcripps was determined from the DC load line. An RC network was then tuned to model S22 from which Cds could be determined. This is illustrated in figure 7 below.

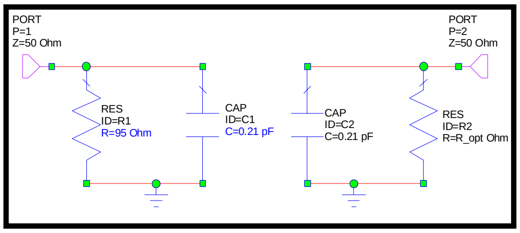

FIGURE 7: RC Network used for Power Match

The reflection coefficient at port 1 of the network on the left of figure 7 determines the optimum power match point. Notice that Rcripps is about 50 Ohms so a single shunt inductor was chosen for the match.

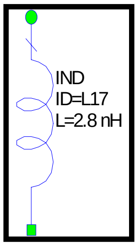

FIGURE 8: Output Matching Network (OMN)

The shunt inductor shown in figure 8 was also used as the DC feed for the drain of the 600um FET.

F. Converting to TQTRx Elements and Interconnects

Each subcircuit was converted an equivalent circuit using the TQTRx elements from the design kit and connected using microstrip lines, tees and crosses. The Microwave Office circuit simulator has an element called MTrace that models the bends when the trace is auto-routed in the layout of the circuit. This eliminated the need for including bends in the circuit. Each converted TQTRx subcircuit is then compared to the corresponding lumped element subcircuit used in the initial design.

IV. SIMULATION RESULTS

Since each TQTRx element in each subcircuit has associated artwork the layout of the subcircuit is automatically generated at the touch of a button. Minor manipulations are required to position connections to other subcircuits.

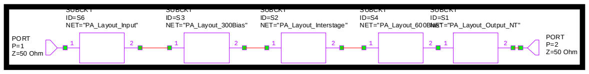

FIGURE 9: Subcircuit-Connected Power Amplifier

When all the subcircuits are connected as illustrated in figure 9 the entire amplifier can be simulated for small-signal and large-signal performance. Table 2 shows a summary of the performance of the amplifier at the two major stages of the design process.

TABLE 2
SUMMARY OF DESIGN SPECIFICATIONS

	Specifications	Pre-Layout	Post-Layout
Amplifier Class	F	AB	AB
Frequency	5150 MHz to 5875 MHz	yes	yes
Bandwidth	>800 MHz	yes	yes
Gain	>13 dB		>22 dB
Gain Ripple	+/- 0.5 dBmax	<0.5 dB	<0.5 dB
Output Power	>+20 dBm @ 1dB Compression	>23 dBm	>22 dBm
Efficiency	>20% @1dB Compression; goal = 25%	>33 %	>30 %
VSWR	<1.5:1 (input, output)	1.2, 1.9	1.2, 2.1
Supply Voltage	+/- 5 volts	+4, +5	+4, +5
Size	60 x 60 mil	NA	yes

The simulated performance of the amplifier was very encouraging. Figure 10 shows the small-signal performance (S11, S22 and S21).

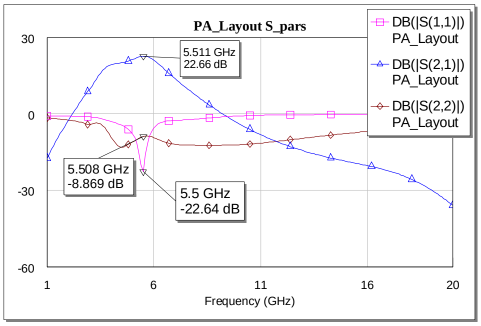

FIGURE 10: Small-Signal Performance of the Final PA

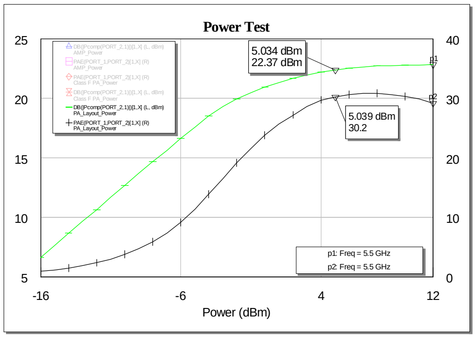

FIGURE 11: Large-Signal Performance of the Final PA

Figure 11 shows the Large-signal performance of the PA. Note that Output Power is displayed on the left y-axis and Efficiency is displayed on the right

V. FINAL SCHEMATIC AND LAYOUT

The final subcircuit schematics of the power amplifier are presented as an attachment (see appendix A) since they are too large to be legible.

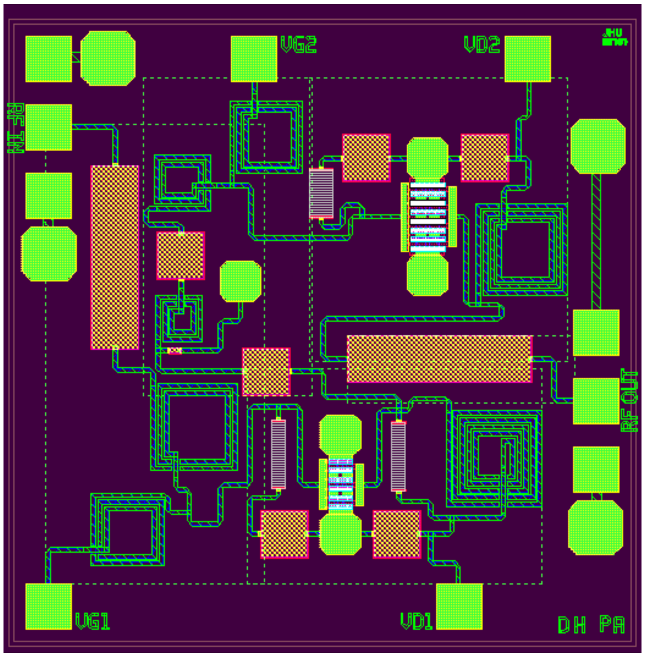

FIGURE 12: Layout of the Final PA

VII. TEST PLAN

In order to measure the amplifier after fabrication it was necessary to place DC and RF pads on all four sides of the chip. DC needle probes will be used to provide individual bias to the gate and drain of each transistor (top and bottom of chip as shown in figure 12). RF probes will come in from the left and right of the chip for input and output, respectively.

VII. CONCLUSION

The overall goals of the design were met, with the exception of the output VSWR. Since this was achieved with a class AB design and the performance was considerably higher than the specifications, the class F design was not necessary for this application. So a chip size trade-off was considered and consequently the class AB design was chosen. With this design It was not necessary to make any other performance trade-offs.

ACKNOWLEDGEMENT

The authors wish to acknowledge the technical support of Applied Wave Research and Triquint Semiconductor for providing the Process Design Kit and fabrication services, respectively.

REFERENCES

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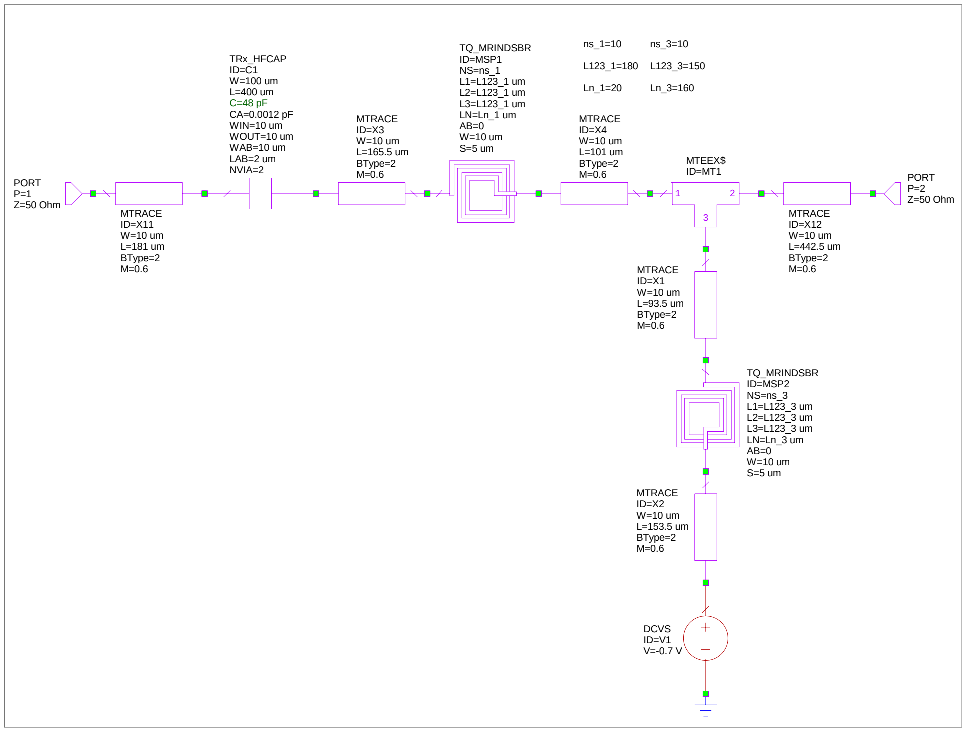
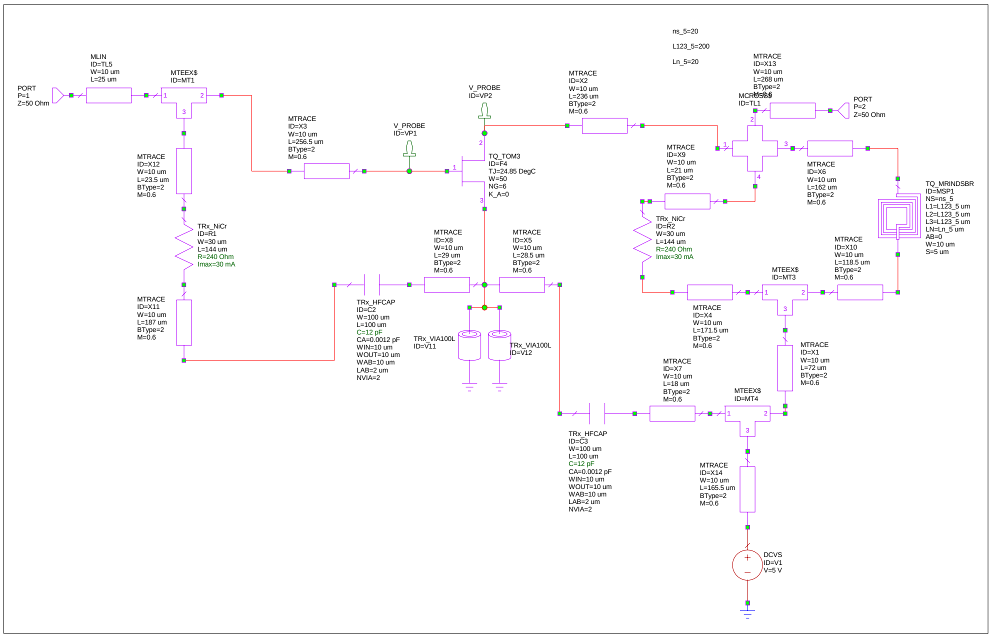
[2] F. H. Raab, “Maximum Efficiency and Output of Class-F Power Amplifiers,” IEEE transactions, Vol. 49, No. 6, June 2001, pp 1162-1166.

[3] C. Moore and J. Penn, “Microwave Monolithic Integrated Circuit Design”, Class Notes, Johns Hopkins University, Fall 2004

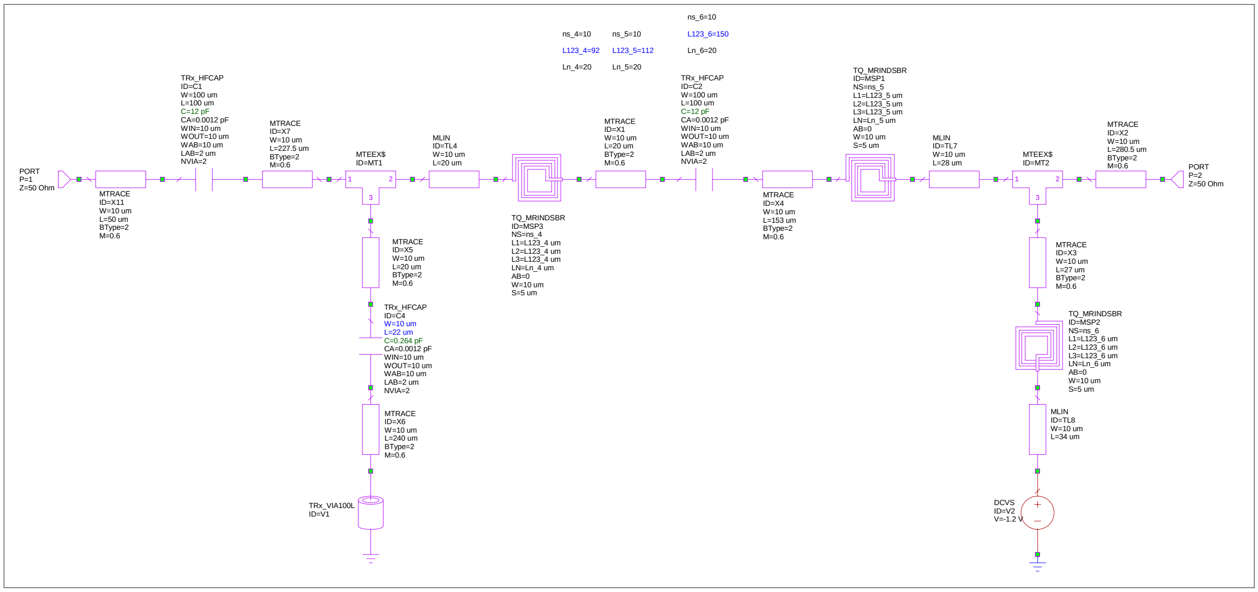
Appendix A



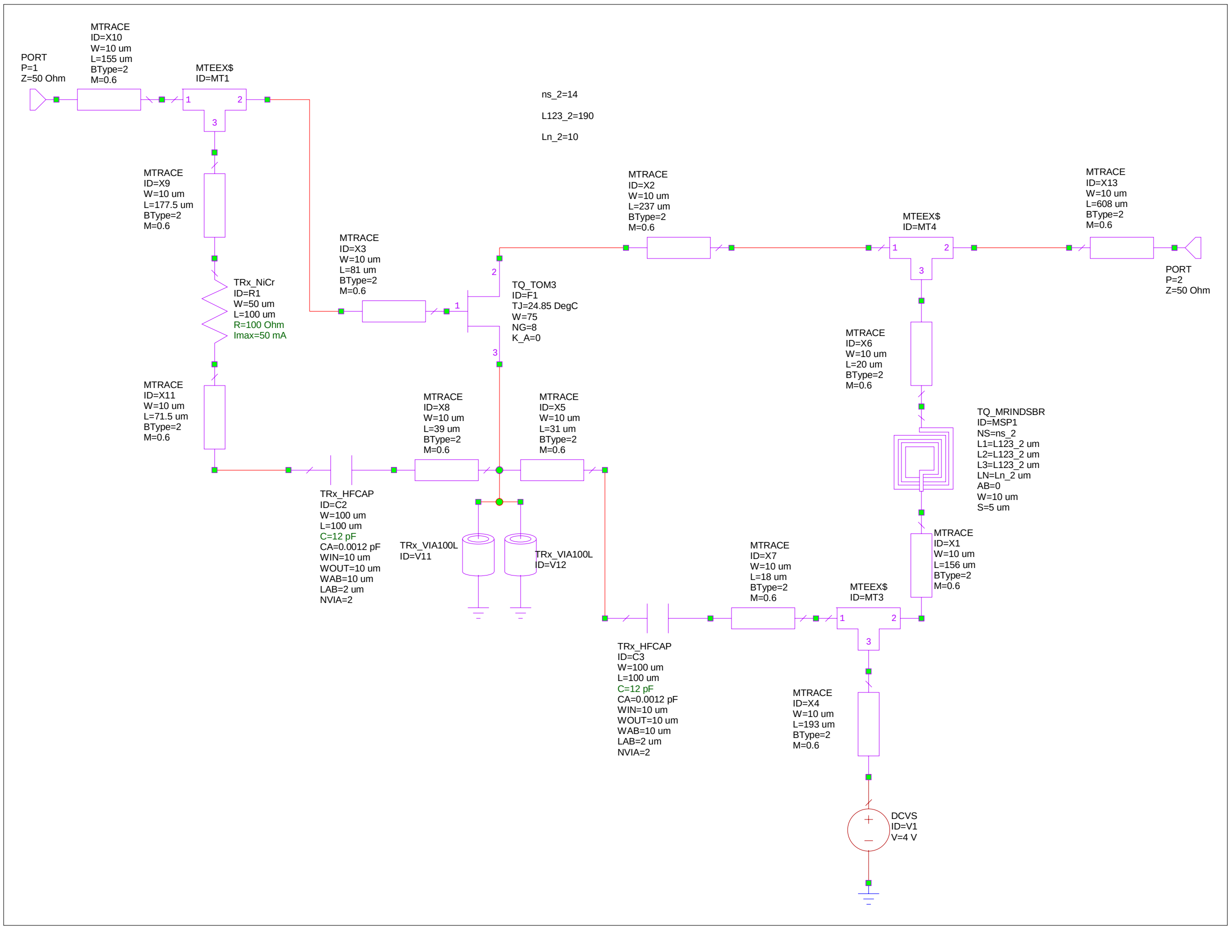
Input Matching Network (IMN)



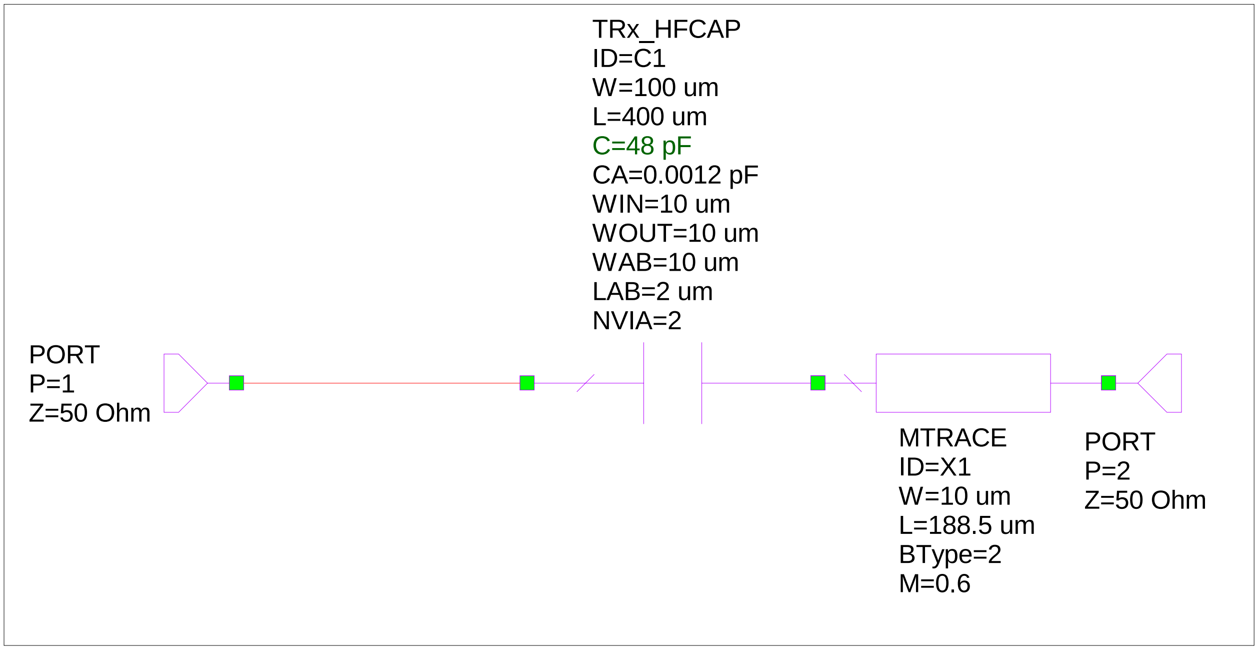
Biased 300um GFET



Interstage Matching Network



Biased 600um GFET



Output Blocking Cap (matching Inductor included in Biased 600um network)