

**A 5.8 GHz MMIC  
Quadrature Modulator  
in GaAs**

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## **Abstract**

This paper documents the design of a Quadrature Modulator in the 5.8GHz Industrial-Scientific-Medical (ISM) Band, using the TriQuint TQS TRx process. The design was completed to fulfill the requirements of the Microwave Monolithic Integrated Circuit (MMIC) Course at The Johns Hopkins University. The modulator was designed using a TriQuint-provided library for Agilent's Advanced Design System (ADS), on a 60x60 mil GaAs substrate. It was designed to be used in a high data rate QPSK transmitter, when combined with other projects designed in the course.

## Intro

This paper documents the design of a Quadrature Modulator in the 5.8GHz Industrial-Scientific-Medical (ISM) Band, using the TriQuint TQS TRx process. The design was completed to fulfill the requirements of the Microwave Monolithic Integrated Circuit (MMIC) Course at The Johns Hopkins University. The modulator was designed using a TriQuint-provided library for Agilent's Advanced Design System (ADS), on a 60x60 mil GaAs substrate. It was designed to be used in a high data rate QPSK transmitter, when combined with other projects designed in the course.

## Circuit Description

The modulator circuit was designed as separate 90° and 180° switchable phase-shifters in series, allowing for a net switchable phase shift of 0°, 90°, 180°, or 270°. The phase-shifters were constructed with a pair of input switching FETs, a phase-delay or bypass path, and a pair of output switching FETs. The phase-shifters run on a bipolar supply of ±5Vdc. Incorporated on-chip are a pair of complementary-output TTL-to-bipolar drivers that allow control of the phase-shifters using standard TTL level logic signals; one driver is needed per phase-shifter. The drivers produce 0 and -3.5V control outputs to the phase-shifters, and operate on ±5Vdc.

## Design Philosophy

The primary goal in designing the modulator is to ensure the proper phase change between the various states, 90° for QPSK. QPSK also relies on a I/Q constellation where each symbol has equal amplitude, thus amplitude matching between the 4 phase states was the secondary design goal. Other important design criteria included allowing TTL control levels, and a sufficient IP3 so as not to compress and introduce higher-order products when driven directly by a 0dBm VCO, since the transmitter system as envisioned has no output bandpass filter.

The first step was designing the two phase-shifters. The 90° shifter uses a single lumped-element  $\lambda/4$  transmission line at the center frequency, while the 180° shifter uses two  $\lambda/4$  lines in cascade; this approach simplified design and simulation since the two shifter were nearly identical. The 90° shifter, being the slightly less complex one, was designed first.

The switching was implemented using the FETs in a switched amplifier topology, with the input applied to the gate, and the output at the drain, using TriQuint 140 $\mu$ m DFETs to provide adequate IP3. This approach provides a very high impedance at the "off" FET, since  $R_{GS}$  is much greater than  $R_{DS}$  in the off state, which improves the isolation. This also provides gain, controllable by a drain bias resistor, compensating for any losses in the delay elements or the chip. Since the signal must pass through four switches, this technique was used, as a traditional drain-source switching system would be lossy itself,

and provide no means to compensate for other system losses. Switching control from the bipolar drivers was provided by a 1.5k $\Omega$  bias resistor at the gate.

The completed 90° shifter had two signal paths: FET-Line-FET, and FET-pad-FET. The line was implemented as a PI-network, with shunt capacitors at input and output, and a series inductor. The pad was used initially to provide amplitude matching between the delayed path and the non-delayed path. It was subsequently removed, and the amplitude match was accomplished by varying the drain bias resistors in both paths until there was less than 1dB of variation over the operating band.

The 180° shifter was designed from the 90° shifter by adding a second  $\lambda/4$  line, and combining the common-node shunt capacitor into a single capacitor for simplicity. Drain resistances were varied to compensate for the additional loss in the longer transmission line, but otherwise the shifters are identical.

When cascaded, the two shifters provided nearly 15dB of small-signal gain, while presenting a poor input VSWR. Since this gain was not necessary according to the original design guidelines, 5dB was sacrificed as input attenuation to provide better than a 2:1 VSWR over the entire operating bandwidth. No complicated matching was necessary. Overall, the system has a nominal gain of 10dB, with an amplitude variation of  $\pm 0.5$ dB between phase states over the operating band.

The TTL-to-bipolar drivers were designed from a reference schematic provided by the course instructor, using 12 $\mu$ m and 18 $\mu$ m DFETs.

### **Trade-offs**

The most significant trade-off was in using the switched-amplifier technique instead of a classic switch. While the classic switch would have consumed less current, initial simulations proved to be too lossy to meet the design requirements. It also would have relied on purely passive amplitude matching, adding to the total loss. A hybrid amplifying/passive switch approach was considered, but it eliminated the symmetry, and made the design more complicated.

### **Modeled Performance**

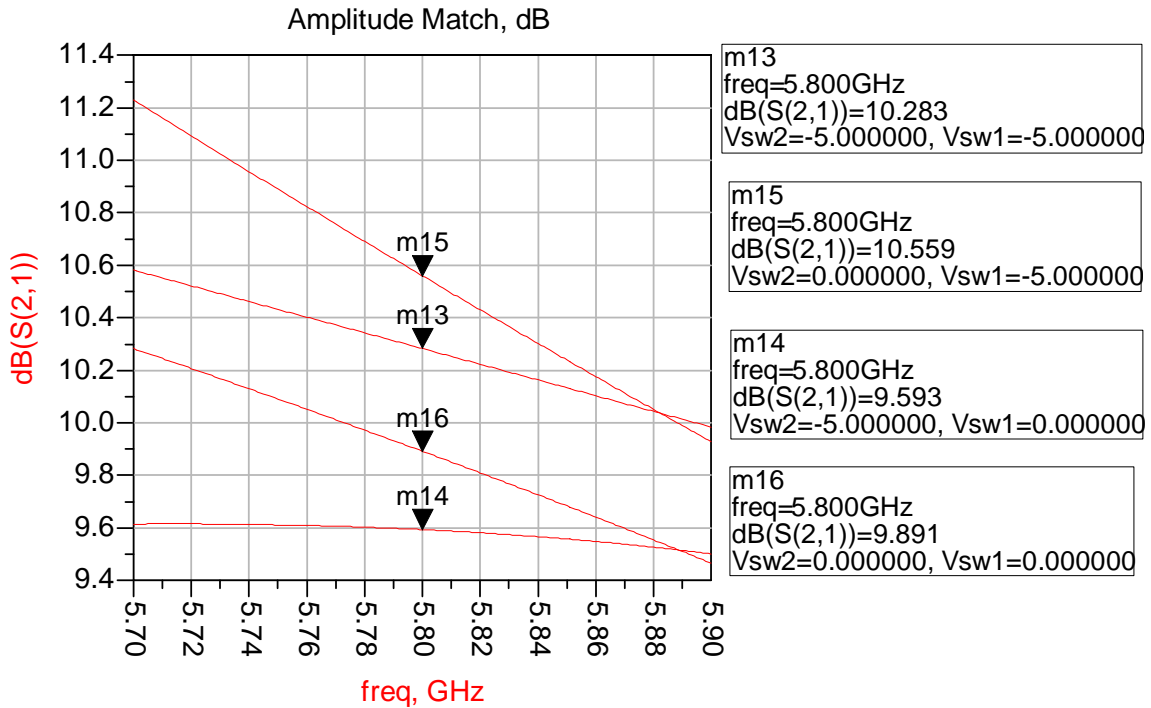
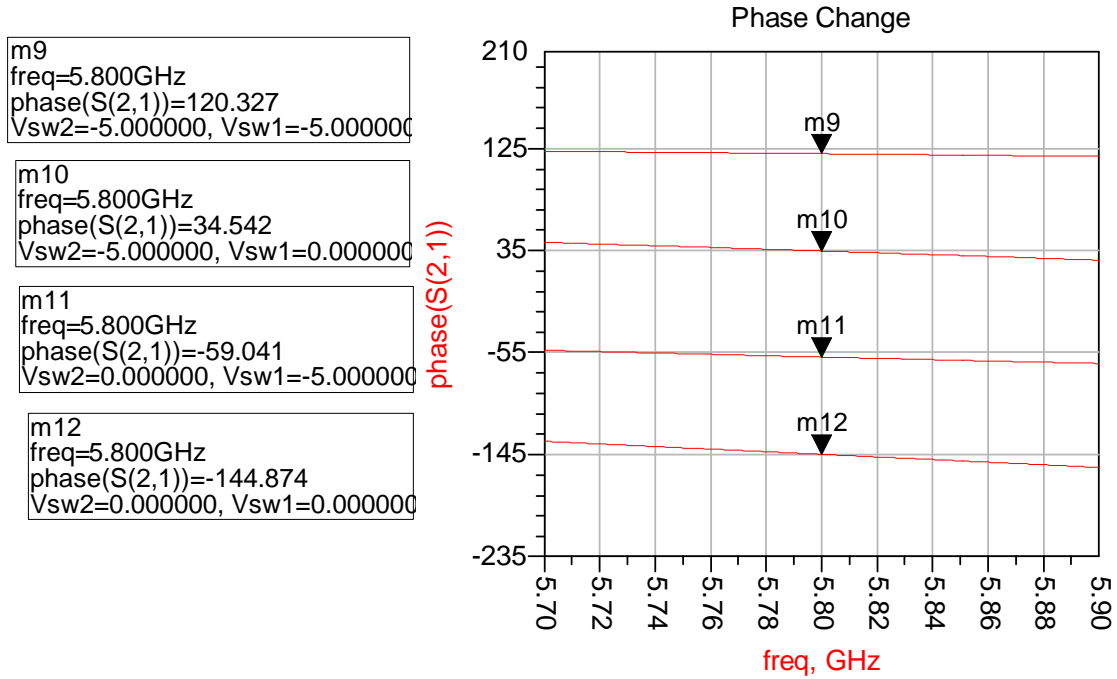
#### **Specifications**

The following table contains the performance specifications for the modulator:

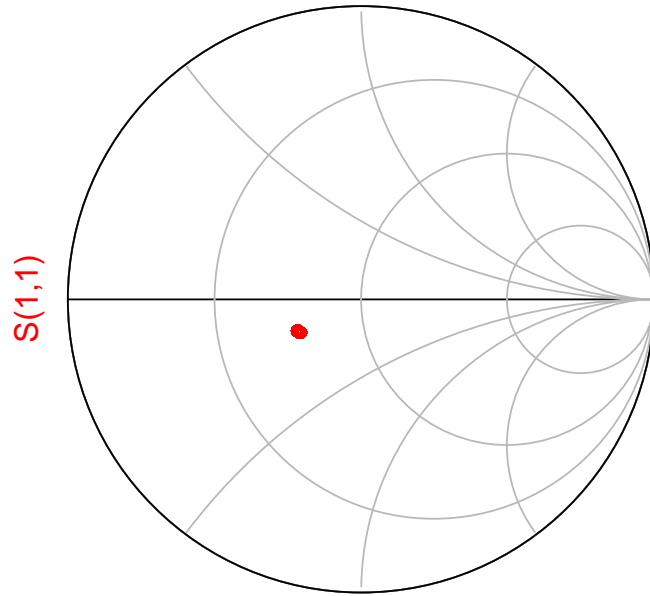
Frequency	5.8 GHz $\pm$ 100 MHz
Vsupply	$\pm$ 5Vdc
Control	+5V TTL
Amplitude Balance	$\pm$ 1dB
Phase Shift	90° $\pm$ 5°
Instantaneous Bandwidth	0 to 20 MHz

## Predicted Performance

Below are plots of the simulated performance. All parameters were met.

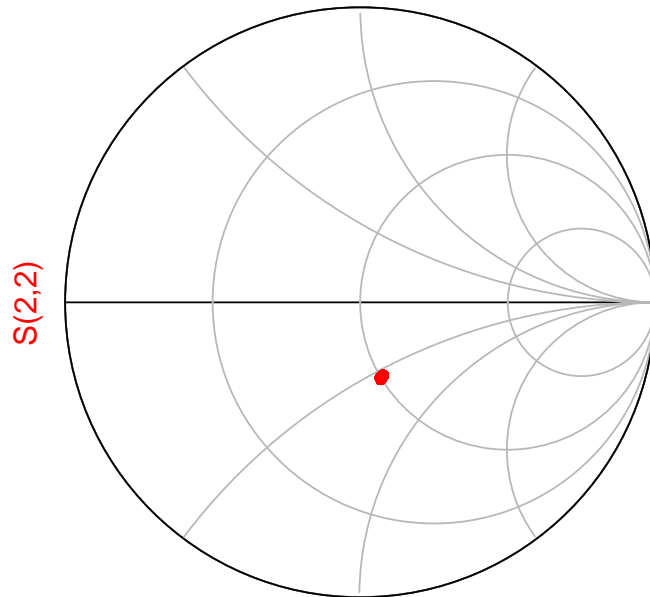


Input Reflection Coefficient



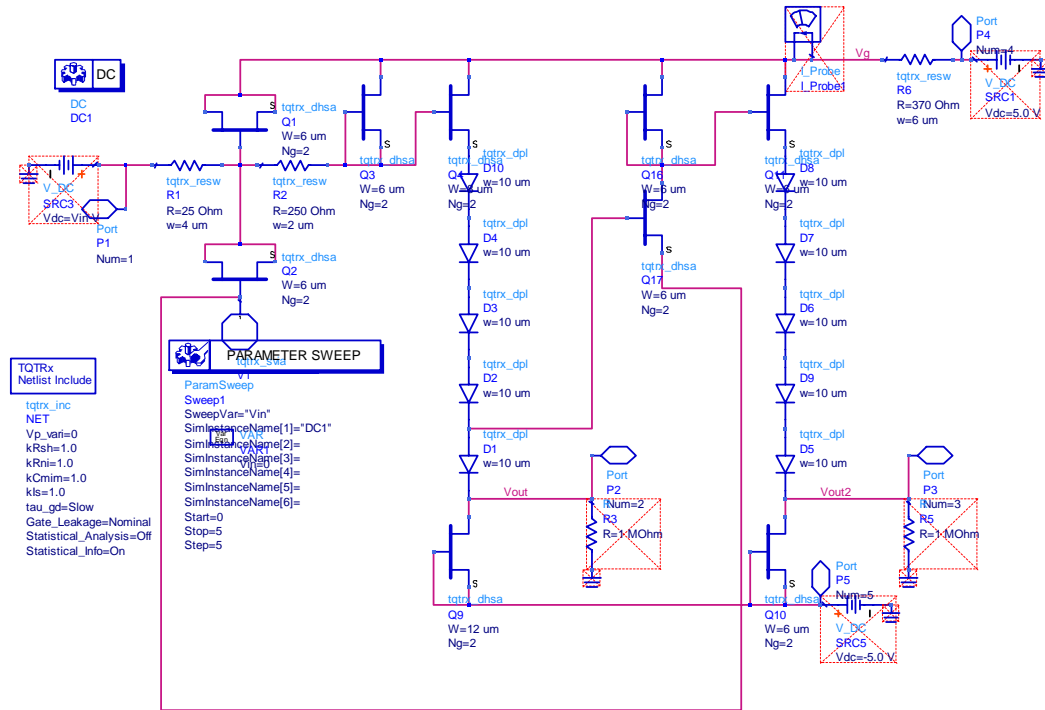
freq (5.700GHz to 5.900GHz)

Output Reflection Coefficient

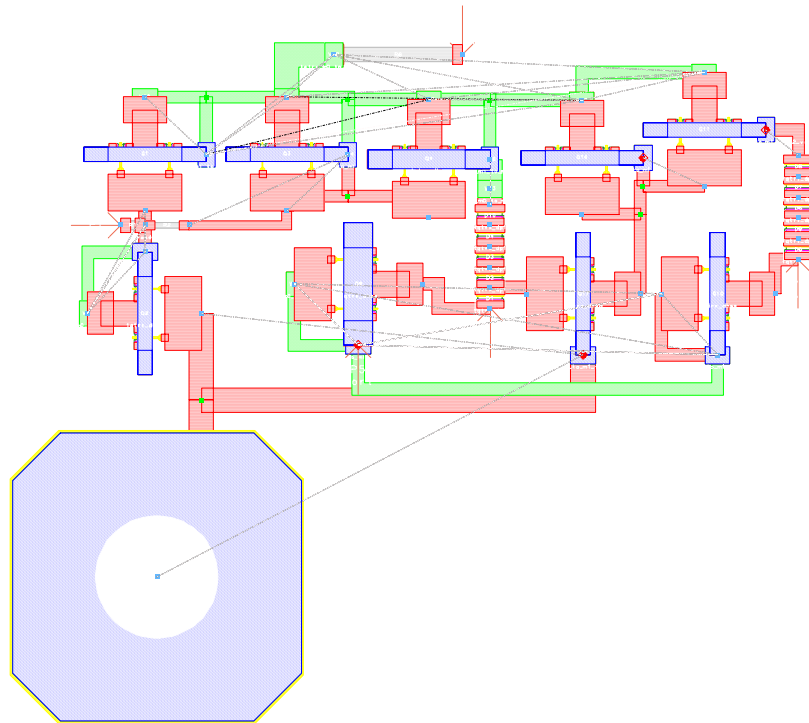


freq (5.700GHz to 5.900GHz)

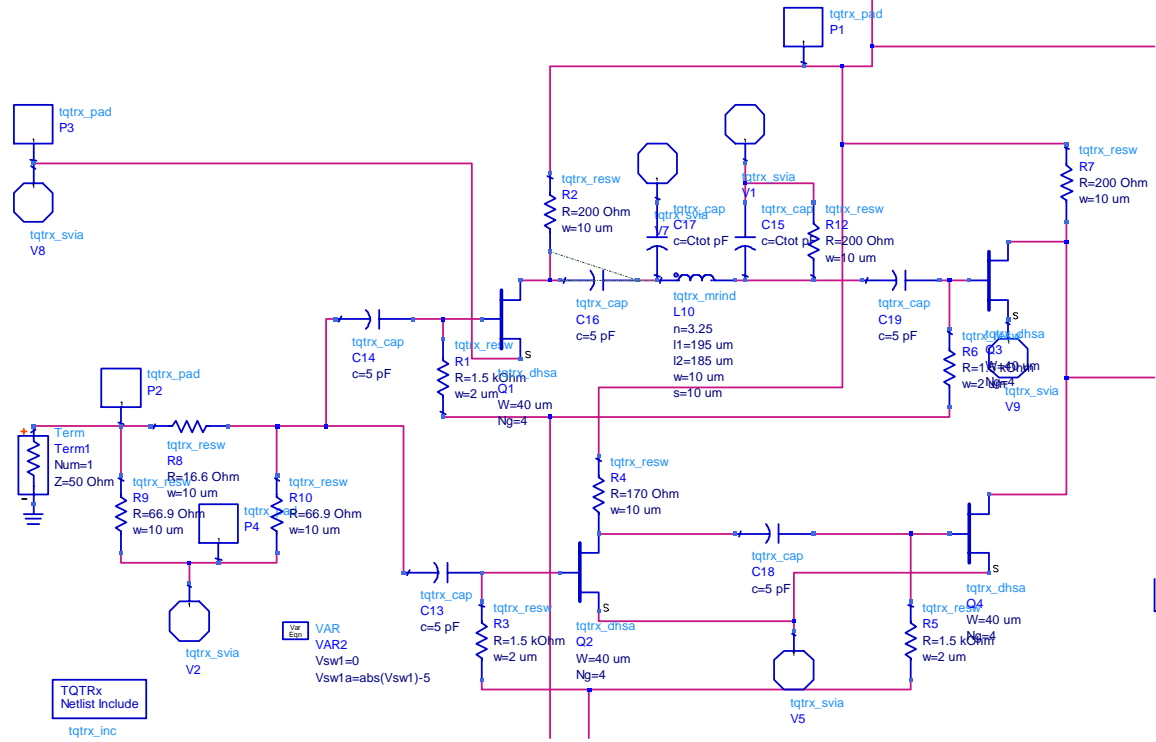
# Schematics



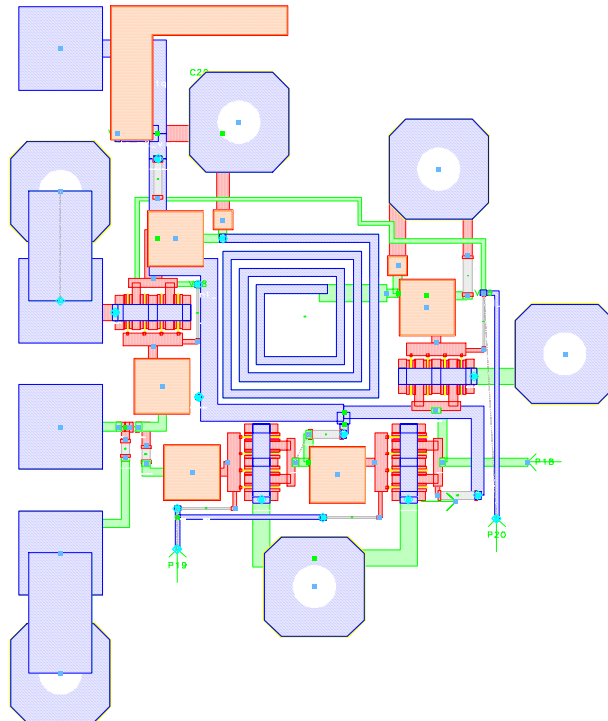
# Driver Schematic



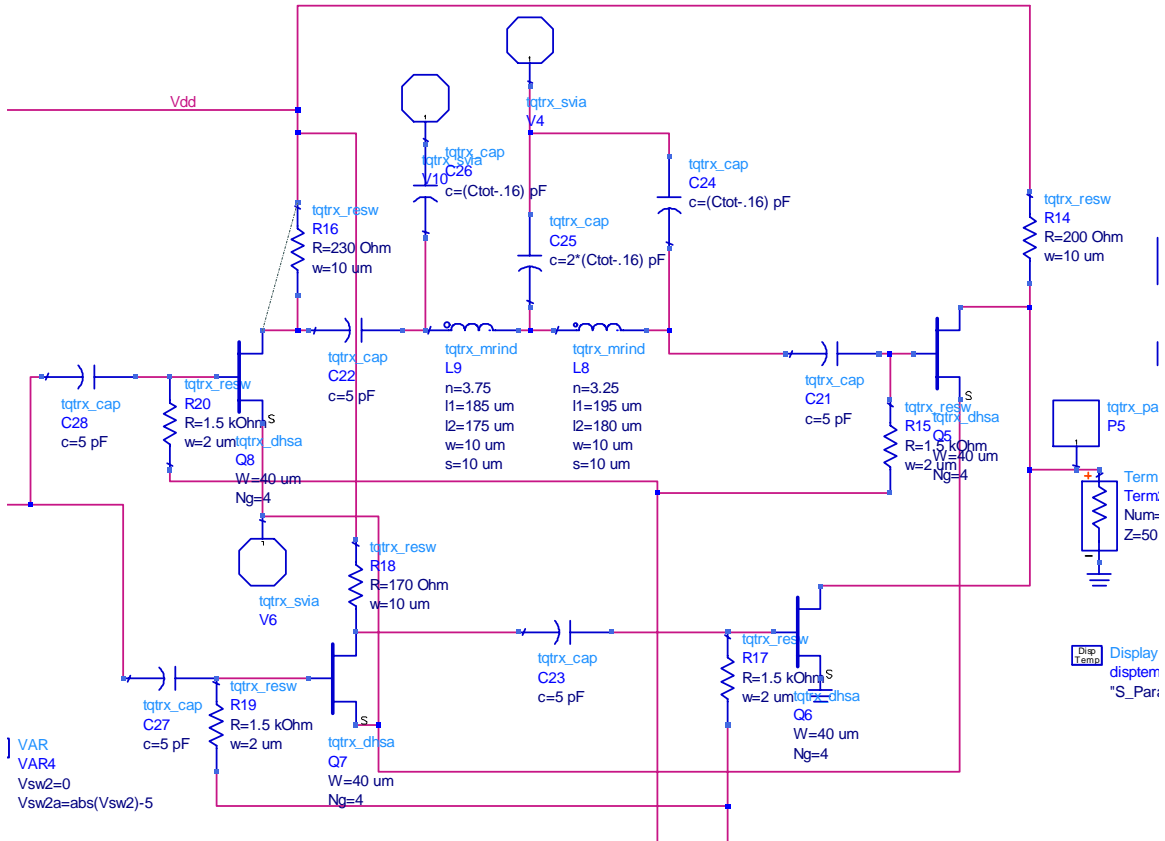
# Driver Layout



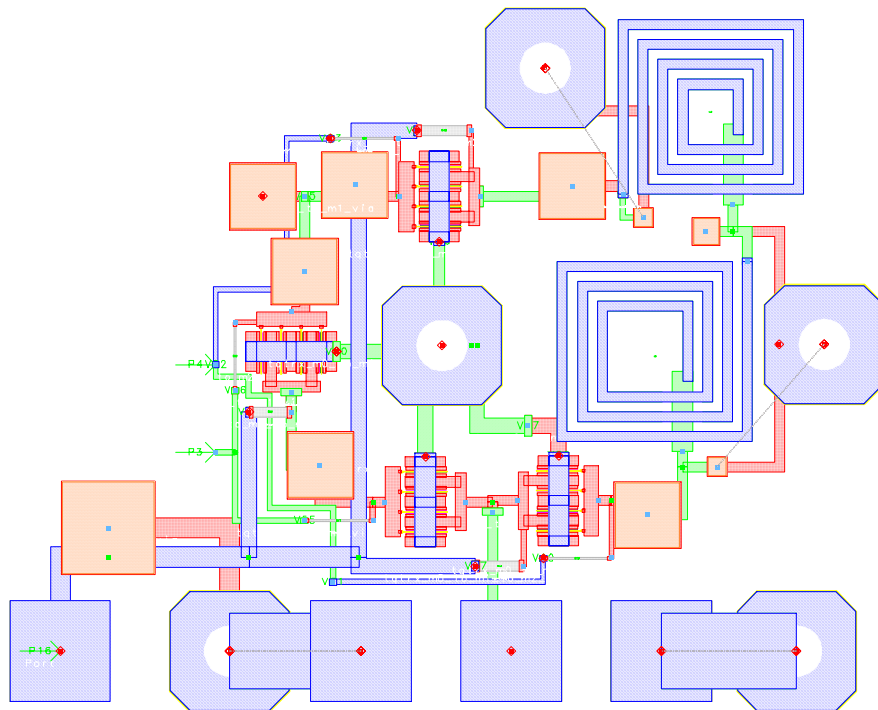
Quarter-Wave Shifter Schematic



Quarter-Wave Shifter Layout



Half-Wave Shifter

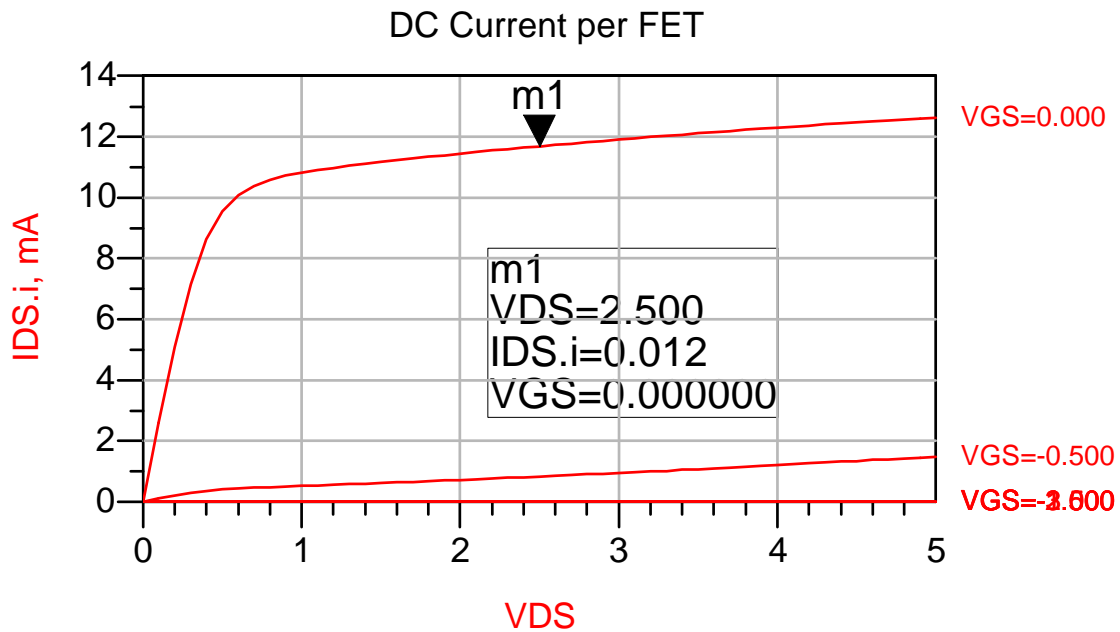


Half-Wave Shifter



## DC Analysis

Total current consumption is approximately 57mA, which is not unacceptable. While a design without gain would have had a lower current, this still meets the design goals.



## Current Consumption (mA)

freq	I_Probe1.i
Vsw2=-5.000, Vsw1=-5.000 0.0000 Hz	57.61mA
Vsw2=-5.000, Vsw1=0.000 0.0000 Hz	57.46mA
Vsw2=0.000, Vsw1=-5.000 0.0000 Hz	57.31mA
Vsw2=0.000, Vsw1=0.000	

## Test Plan

The following equipment is required for test:

- $\pm 5$  Vdc supply
- Spectrum Analyzer
- RF Signal Generator
- Function Generator (x2, phase locked), for control signals
- Vector Signal Analyzer **or** Quadrature Demodulator
- Oscilloscope

Proper power sequencing must always be followed; ensure grounds are connected, then connect the -5 Vdc and then +5 Vdc. Next, connect the function generators to the control inputs, with a square wave output at the modulation frequency, and levels of 0-5V. Use the oscilloscope to adjust the relative phase of the generators to approximately  $90^\circ$ , this will create modulation that will rotate the output constellation.

Connect the RF signal generator to the input at the desired frequency, with a power level of 0dBm. Connect the vector signal analyzer to the output, and configure it for a QPSK modulation. The constellation should now be visible. Alternatively, connect the quadrature demodulator to the output of the MMIC, and connect the I and Q signal to the oscilloscope, set in X-Y mode. After adjusting the holdoff on the trigger, the QPSK constellation should be visible.

Measure the relative phase and amplitude of the four constellation points to ensure they are within 1dB relative amplitude, and  $90^\circ$  phase rotation. Next, connect the spectrum analyzer to the output, and measure the output power; compute the gain. Last, open the spectrum analyzer's span to check for high-order mixing products.

## Conclusions and Recommendations

The modulator design and layout appear successful. The next step would be to create an actual I/Q mixer to allow higher-order modulations, such as 16QAM, or 8OFDM to be used.