

MMIC Design
EE787

Post Amplifier

Authors:
Henry Jeffress
Jay Walters

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Table Of Contents

Abstract

Introduction

 Circuit Description

 Design Philosophy

 Trade-offs

Modeled Performance

 Specification Compliance Matrix

 Predicted Performance

Schematic Diagrams

DC Analysis

Test Plan

 Linear Parameters

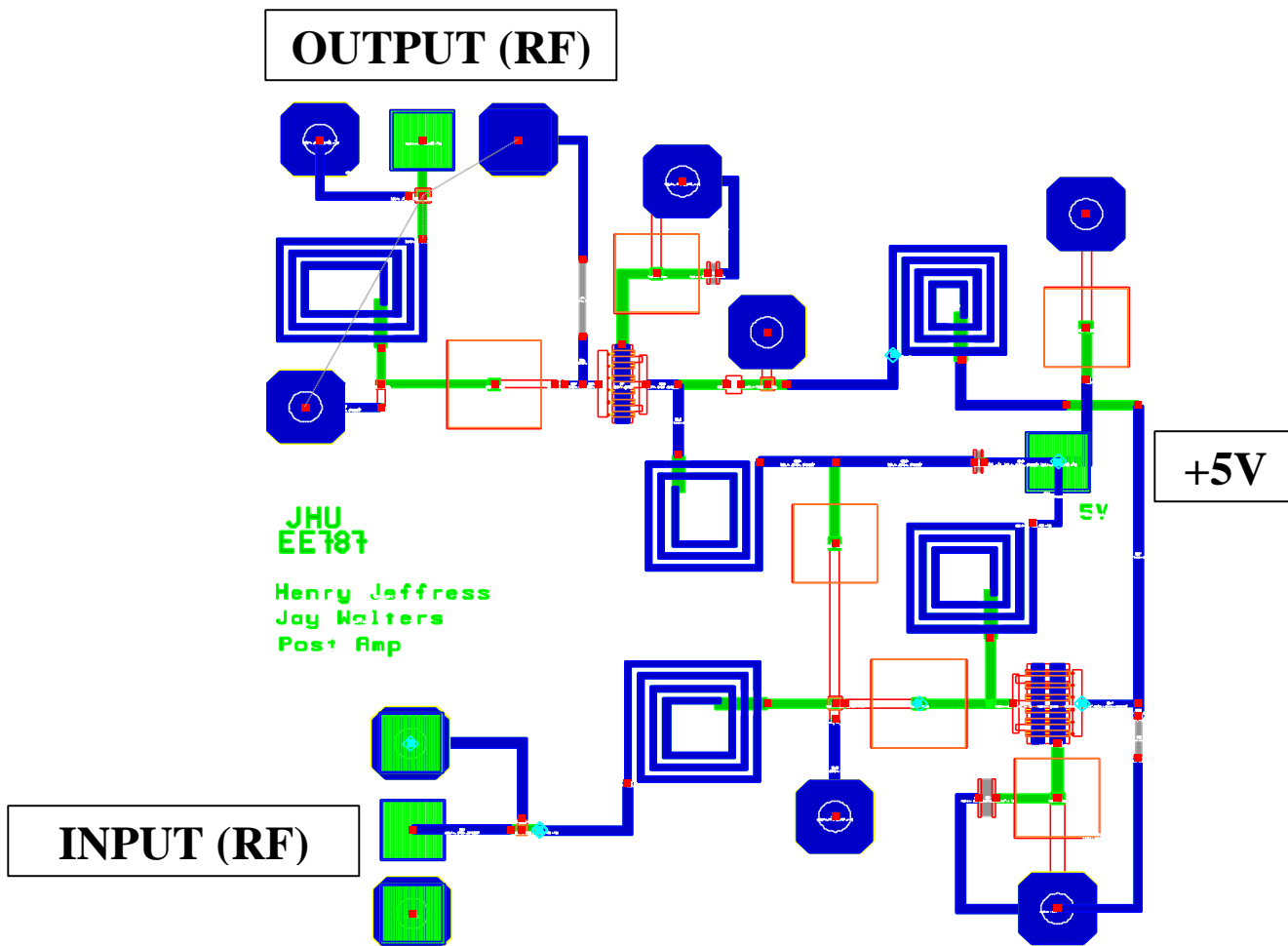
 Power Measurements

Conclusion & Recommendations

ABSTRACT

This report documents the design of a post amplifier for use as part of a simplex transceiver for the C-band industrial, scientific, and medical (ISM) band. More specifically, the post amp is design to work primarily from 5.725 Ghz to 5.875 Ghz, which is a 0.15 Ghz bandwidth. For the manufacturing of our post amp we will be using a Triquint Trx process.

The Post Amp design was simulated using Agilent's Advanced Design System 2003C (ADS) software using elements based upon Triquints process. The layout was also done using ADS using a 60 x 60 mil AnaChip.



INTRODUCTION

Circuit Description

The circuit topology selected for the design was a cascaded two-stage amplifier layout requiring only one power supply. The matching networks were designed using lumped element topology.

Design Philosophy

The Post Amplifier needed to be designed with a minimal gain of 15 dB. We used this specification to first determine that we needed more than one stage. A simple analysis was run on Gfet's at different gate widths in order to determine the MaxGain of the device. This will allow the determination of the gate sizes for each stage in order to obtain the required gain. It was found that using a 200 micron GFET for the first stage and a 400 micron GFET at the second stage would give us more gain than needed which would allow room to sacrifice gain for a better match.

The first step in designing the post amplifier was to determine where the device should be biased. Determining this is simply done by using ADS's Amplifier=> DC and Bias Point Simulations => and FET IV Curves template. For maximum gain, we already had in mind that we wanted to bias the device at $IDSS / 2$. By correctly using the template, we determined that we wanted to bias the first stage at:

$$I_{ds} = I_{dss}/2 = .028mA = 28.0 \text{ } \mu\text{V} = V_{ds}, -.88 \text{ V} = V_{gs}$$

And the second stage at:

$$I_{ds} = I_{dss}/2 = .056mA = 56.0mA @ 5 \text{ V} = V_{ds}, -.88 \text{ mV} = V_{gs}.$$

The next step in the design was to determine the input and output matching circuitry for the first and second stages separately. With the Cripps method in mind, this process was accomplished through the use of ADS's built in SmGamma1 and SmGamma2 functions. These functions return the simultaneous match input and output reflection coefficients. Once these were determined we used the small utility "smith.exe" to determine the matching network that would translate the match of our design to the Gamma's calculated by ADS. This produced very accurate input and output matching networks.

Upon completion of the matching networks for each stage, both stages were optimized for optimal gain, output power, and return loss. The results were analyzed using both linear and nonlinear simulated data. The two separate stages were then combined and the overall performance of the amplifier was optimized. After satisfactory performance was obtained using the ideal elements in the combined two-stage design, the ideal elements were replaced by Triquint elements. Special attention was given to the size of the Triquint elements, especially the inductors, which have been shown to be lossier than ideal inductors. The final stage of the design process was to generate a layout of the circuit that was just simulated. Considering the layout of each element during optimization was extremely helpful during the layout process. All elements were placed such that they fit withing the 60 x 60 mil Anachip and that isolation and crosstalk were

minimized. Another consideration with the layout was that of power-handling of elements and traces. Where applicable elements were enlarged and traces widened to be able to handle the current. This was only an issue in the DC Bias path. Once the layout is complete, the simulation was tweaked to add all the new element values, microstrip lines, tees, and vias and re-simulated to make sure performance was still acceptable.

Trade-offs

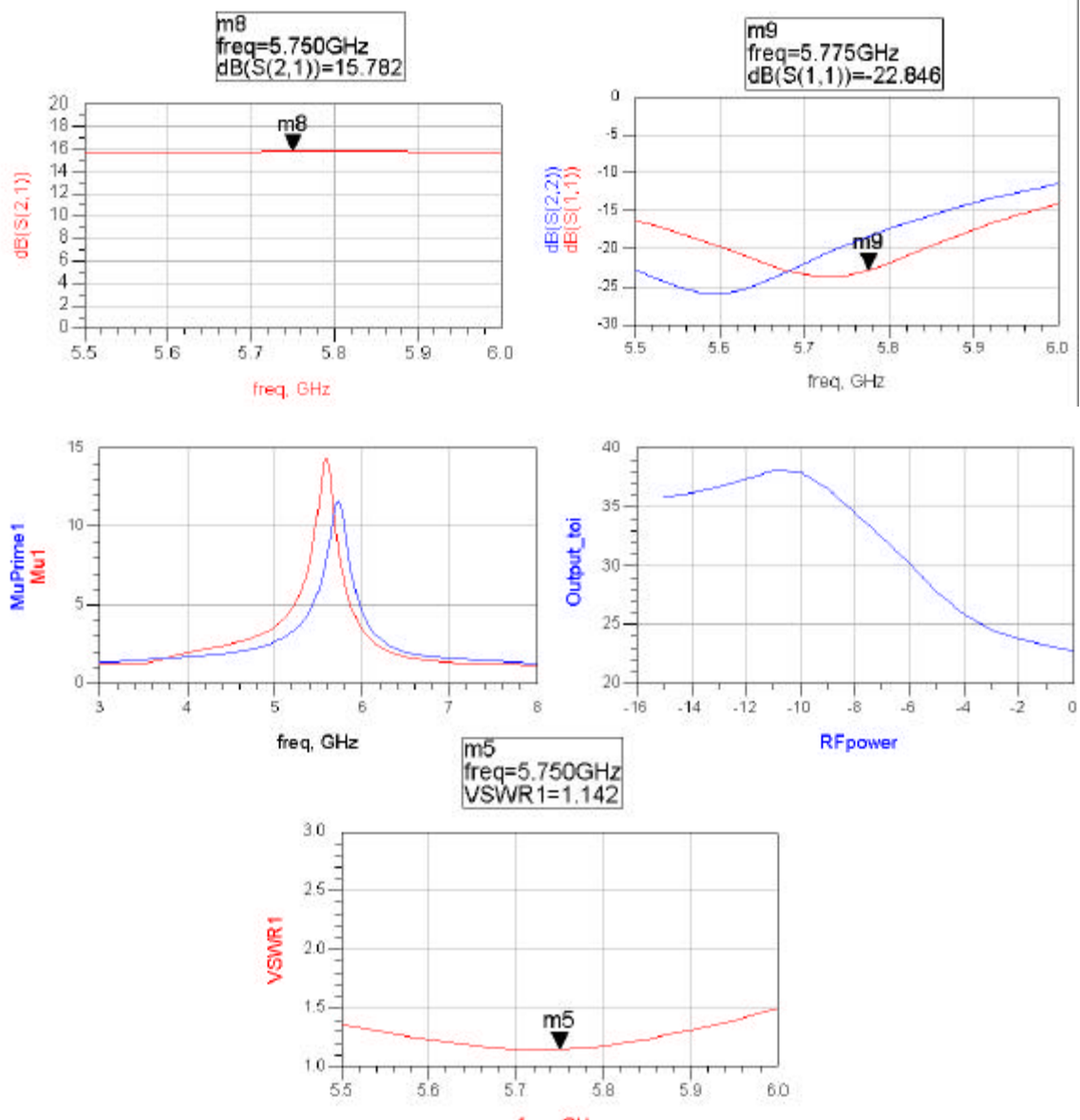
As with any design this C-Band Post Amplifier design had a couple of trade-offs. However, the ability to design the Amplifier utilizing just one power supply increased the efficiency of the design from a layout standpoint (less biasing inductors) and allowed us a great deal more versatility in the layout. Of course, nothing is perfect and sacrificing one spec. to achieve another is commonplace. The Gain, IP3, and VSWR performance were all sacrificed at some point to obtain the ideal balance between the three while still maintaining the requirements.

Modeled Performance

| | Goal | Triquint Simulation | Final Layout Schematic |
|----------------------|----------------------------|----------------------------|-------------------------------|
| Frequency | 5725 to 5875 MHz | 5725 to 5875 MHz | 5725 to 5875 MHz |
| Bandwith | > 150 MHz | > 500 MHz | > 500 MHz |
| Gain | > 15 dB | > 18 dB | > 15 dB |
| Output IP3 | > +15 dB | > +25 dB | > +22 dB |
| VSWR, 50 Ohms | < 1.5 : 1 input and output | 1.5:1 input and output | < 1.5 :1 input and output |
| Gain Ripple | +/- 0.5 dB | +/- 0.25 dB | +/- 0.5 dB |

Predicted Performance

Small Signal Characteristic Performance



Test Plan

The following items and test procedures are recommended to test the C-band post amplifier

Linear Parameters

Equipment: Vector network analyzer (Agilent 8510)
Probe Station
Bias Supply

Procedure:

- Calibrate the network analyzer from 0.45 to 15 GHz
- Place the bias probe on the pad of the chip labeled “+5V”
- Place probe tips on the designated pads. The input port is labeled “INPUT” and the output port is labeled “OUTPUT”.
- Turn on the two power supplies.
- Record data.

Power measurements

Equipment: Signal Generator
Spectrum Analyzer

Procedure:

- Connect the signal generator probe to the input pad of the amplifier chip, which is the port marked “INPUT”.
- Connect the spectrum analyzer probe to the output pad of the amplifier chip which is the port marked “OUTPUT”.
- Place the bias probe on the pad of the chip labeled “+5V”.
- Power supplies.
- For P_{in} vs. P_{out} set the generator to the frequency of interest and sweep the power up to, but not exceeding, 10 dBm.
- Record the measurements from spectrum analyzer after each interval.

Conclusion & Recommendations

In conclusion the C band post amplifier design was a success and met and exceeded all of the specification goals. Being able to design the post amp using just one power supply increases the complexity of the design and layout but makes the post amp more robust and easier to test and incorporate into the larger system, in this case the C-band transceiver.