

The Second Swing at Controlled Instability

An  
L – Band VCO

Center Frequency = 1120 MHz  
Bandwidth = 100 MHz

A Student Project Designed By  
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For  
The Johns Hopkins University – Applied Physics Laboratory  
Class # 525.801 – Special Project I:  
Monolithic Microwave Integrated Circuit Design

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## *ABSTRACT:*

This paper describes the re-design of an L-Band voltage controlled oscillator, VCO. The original VCO design<sup>1</sup> was a student's final project in the Johns Hopkins University Monolithic Microwave Integrated Circuit, MMIC, class numbered 525.787. This VCO semester project will identify and correct the problems of the first design. The VCO was design with the Agilent's Advanced Design System, ADS, version 2003A. The VCO's target of fabrication is TriQuint Semiconductor's Texas 0.6 Gallium Arsenide facility. The VCO performance parameters include: center frequency of 1170 MHz; a tuning range of +/- 50 MHz; minimum output power of +10 dBm, desired output power of +13 dBm; supply voltage of +/- 5 volts, desired supply voltage of + 5 volts only, tuning voltage 0 – 5 volts; output impedance 50 ohms, nominal; and sized to fit on the 60 x 60 mil TriQuint ANACHIP.

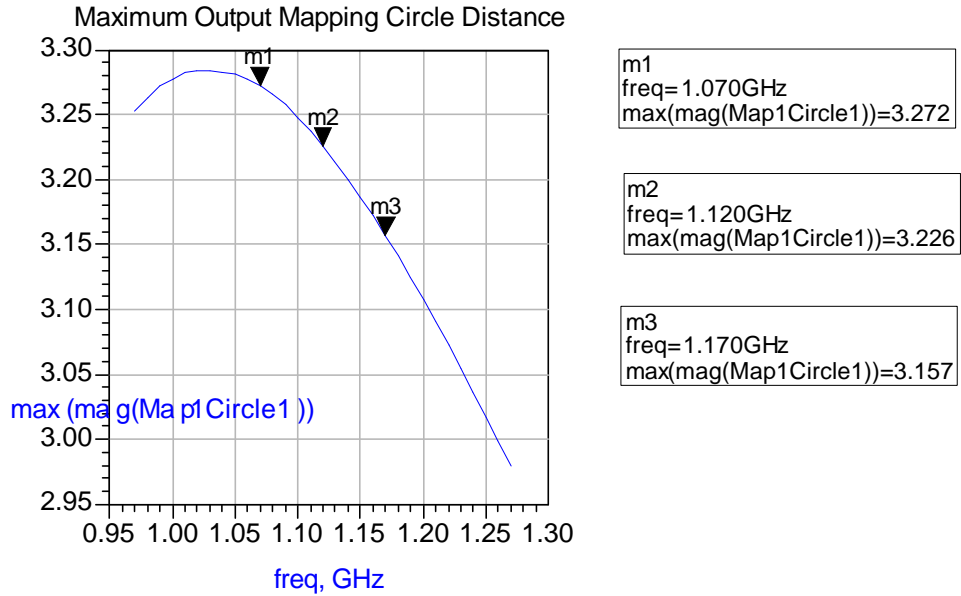
## *DESIGN INTRODUCTION:*

The original VCO's design is a parallel resonator connected to a common source amplifier. Therefore, this re-design effort will continue to use a common source amplifier. A parallel resonator at the gate input determines the frequency of oscillation. A second parallel resonator serves as a high impedance current supply to the amplifier FET's drain. An output matching network converts the high impedance FET output to a nominal 50 ohms. The frequency determining parallel resonator is comprised of two diode connected GFET devices as the voltage controlled variable capacitor and a MRIND inductor, a physical size defined inductor element. A single common source GFET amplifier provides the circuit's gain. The common source MESFET VCO design is uncommon. The bipolar device equivalent design, the common-emitter VCO is also uncommon. The common emitter (source) VCO has fabrication issues stemming from large capacitor and inductor values and performance issues due to the Miller effect because neither the base nor the collector is grounded, Rogers and Plett<sup>2</sup>. However, the design was shown functional at the MIC level, discrete devices mounted on a printed circuit board, by Edwards<sup>3</sup>.

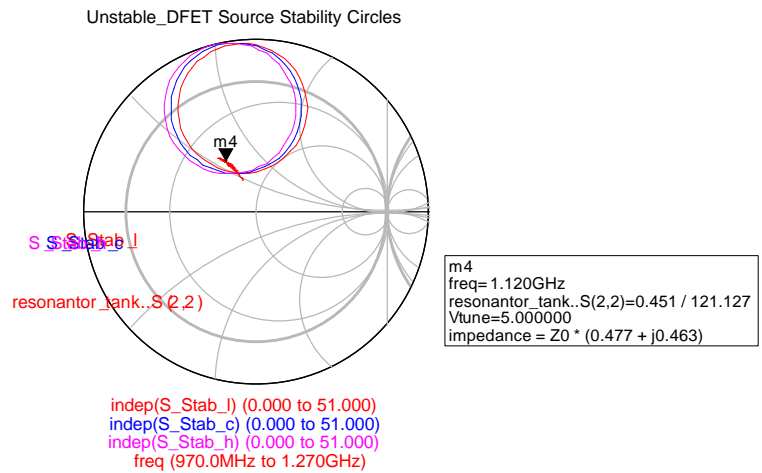
The design methodology starts by adding source resistance to an active device, in this case a MESFET, to create instability. The amount of instability is measured by the parameter maxMP2, the maximum value of the output mapping circle, Edwards<sup>3</sup>. Tune the source resistance until maxMP2 equals approximately 3 at the desired frequency. The parameters maxMP1 and maxMP2 equal the algebraic inverse of the corresponding  $\mu$  stability parameters. The  $\mu$  and  $\mu'$  stability parameters are quantitative figures of merit for the stability of an amplifier, Edwards<sup>4</sup>. Thus, it stands to reason that their algebraic inverses maxMPx are figures of merit for the instability of an amplifier. Now connect a resonator circuit to the input of this appropriately unstable amplifier.

Determine maxMPx from simulations executed on a biased FET device. This includes the parallel resonator current supply and the external gate to source feed back capacitor, Cgs. Also, include a source resistor bypass capacitor of reasonably low impedance, from five to ten ohms.

Below is a graph of maxMP1, the maximum distance from the center of the smith chart to the edge of the output mapping circle. The markers indicate the upper, lower, and center points of the frequency range. Marker dialog boxes, right, indicate the exact value of the maxMP1 function.



Once an adequately unstable, and biased device, is configured, design the input resonator circuit for the frequency range of interest. To insure that these circuits match, plot the output reflection coefficient, S22, of the resonator circuit and the source stability circles of the unstable biased FET circuit on the same smith chart. Design the resonator such that S22 is positioned inside the source stability circles.



Next design an output matching circuit, and tweak achieve the desired frequency.

*SIMULATION SUMMARY:*

Specifications Compliance Matrix for Original L-Band Voltage Controlled Oscillator

	Specification	Pre-Layout	Post-Layout	Fab'ed IC
Frequency Range	1070 to 1170 MHz	1056 to 1171 MHz	1012 to 1156 MHz	1005 to 1155 MHz
Output Power	> +10 dBm > +13 dBm goal	~ +19 dBm	~ +19 dBm	~ +18.5 dBm
Control Voltage	0 to 5 Volts	0 to 2 Volts	0 to 0.5 Volts	0 to 0.5 Volts (Sometimes)
Supply Voltage	± 5 Volts. Goal - +5 Volts only.	Single +5 Volt Supply	Single +5 Volt Supply	Single +5 Volt Supply
Output Impedance	50 Ω, nominal	50 Ω, nominal	50 Ω, nominal	Untested
Size	60x60 mil ANACHIP	N/A	Fit	Fit

*TEST SUMMARY:*

The VCO output frequency ranged from 1.005 to 1.155 GHz, approximately 50 MHz below simulations and 70 MHz below the specified range. The output range is sufficient to cover the specified parameter, 100 MHz. The 5 volt single supply bias current measured 74 mA, 10% below simulations. The measured output power, 18.5 dBm, (include 0.5 dBm of cable loss) was 0.5 dBm less than expected. The low 2<sup>nd</sup>, 3<sup>rd</sup>, and 4<sup>th</sup> harmonic power levels indicate a clean sinusoidal signal. The second chip's functionality repeatedly ceased when the tuning voltage exceeded 3.3 volts. This failure, collapse of the oscillator's amplitude, mirrored the intermittent simulation failures seen while tuning the final design.

*TEST DATA:*

Chip 1:VTune (V)	Freq (GHz)	Power dBm	P(h2) dBm	P(h3) dBm	P(h4) dBm
0.0	1.005	17.8	-40.0	-19.3	-25.5
0.5	1.012	17.8	-42.0	-18.2	-24.5
1.0	1.036	18.0	-41.2	-17.5	-23.3
1.5	1.058	18.0	-36.8	-18.3	-22.7
2.0	1.084	17.7	-34.2	-21.2	-23.7
2.5	1.113	17.0	-32.8	-25.3	-25.7
3.0	1.133	17.0	-29.8	-26.5	-25.7
3.5	1.142	16.8	-29.0	-27.8	-25.7
4.0	1.147	16.8	-28.7	-28.3	-25.8

4.5	1.151	16.7	-28.0	-28.5	-25.5
5.0	1.155	16.7	-27.8	-28.7	-25.3

Chip 2:VTune (V)	Freq (GHz)	Power (dBm)	P(h2) (dBm)	P(h3) (dBm)	P(h4) (dBm)
0.0	1.008	17.3			
0.5	1.014	18.0			
1.0	1.038	18.0			
1.5	1.060	18.0			
2.0	1.085	17.5			
2.5	1.114	16.5			
3.0	1.133	16.2			
3.3	1.138	15.7			

Stops Oscillating VTune > 3.3.

*IDENTIFIED PROBLEMS:*

Frequency range offset 50 MHz low:

- 1) A possible source of this offset is that some parasitic capacitances and inductances of elements in the resonant tank were not included in the respective device models, resulting in simulated frequency incorrectly high. Since, other classmate's designs agreed well with their respective simulations, incomplete parasitic modeling has low probability as the source of the error.
- 2) Another possibility is that the fabrication process yielded elements at the extreme or outside their tolerances. Since, other classmate's designs agreed well with their respective simulations, extreme fabrication process variance has a low probability as the source of the error.
- 3) Simulations indicated that small changes in either the absolute value of the Cgs or in the ratio of the Cgs to the source resistor's bypass capacitor, typically induced oscillator frequency shifts. There is a high probability that the design's need for Cgs in absolute terms led to the frequency shift.

Oscillation collapse with high Vtune:

- 1) The, parallel resonator, current supply for the FET amplifier is centered at an incorrect frequency, and may have insufficient bandwidth to cover the entire frequency range with a high enough impedance for the FET's output. This concept has a fair probability of contributing to the oscillator collapse due to three factors.

- A. The element values of this resonant tank are  $C = 10.1 \text{ pF}$  and  $L = 2.0 \text{ nH}$ . Inserting the values into the resonance equation,  $f_0 = \frac{1}{\sqrt{2p\sqrt{LC}}}$ , yields an ideal resonant frequency of  $f_0 = 1.1198 \text{ GHz}$ . The fabricated elements contain parasitics which do alter their frequency responses.
- B. The unloaded  $Q$  of a parallel resonator varies with  $C$  and inversely with  $L$ , equation 6.18 Pozar<sup>5</sup>, as shown in the following equation.  $Q = \omega_0 \frac{2W_m}{P_{loss}} = \frac{R}{\omega_0 L} = \omega_0 RC$ . Where  $W_m = W_e$  at resonance. So, the low inductor value, and the high capacitor value yield a high  $Q$  resonator, which has little bandwidth.  $BW = 1/Q$ , equation 6.21 Pozar<sup>5</sup>.
- C. The oscillator's output frequency is incorrect. Therefore, the high impedance of the current supply occurs at an incorrect frequency.
- 2) A within allowable parameter process variation created a larger variance for  $C_{gs}$  than the design's small tolerance. This idea also has a fair probability of contributing to the oscillator collapse. As previously discussed, the design tolerance for  $C_{gs}$  is very small.
- 3) The amplifier needs more gain. More gain from the amplifier could conceivably overcome the other two mentioned design weaknesses.

#### *RE-DESIGN STRATEGY:*

Correct the output frequency range:

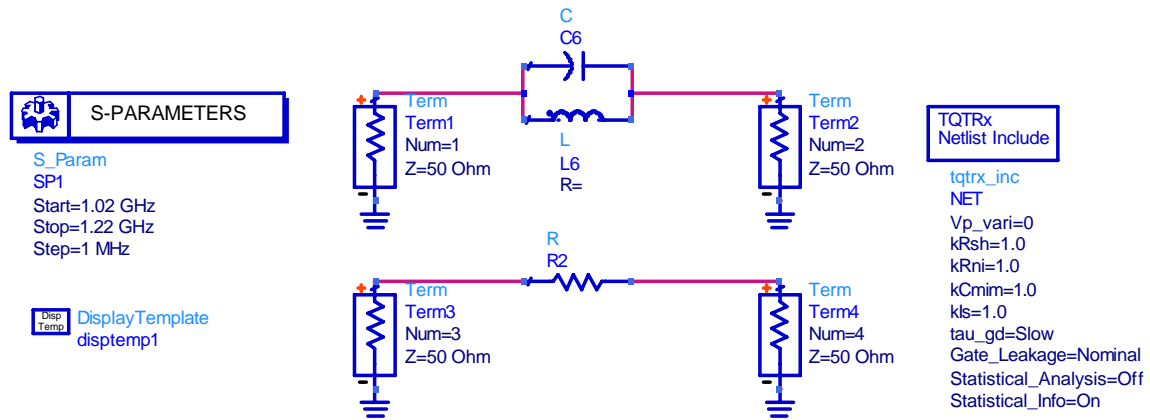
The simulation results of the post-layout circuit, listed in the Specifications Compliance Matrix, align closely with the tested results. To increase the frequency range, raise the frequency of the resonance tank. Because the capacitance in the resonant tank is set primarily by the varactors, the diode connected FETs, increase the resonance tank frequency by reducing the inductor's value. As with the original design, tweak this inductor value to tune the final output frequency when the other changes are complete.

Improve the bandwidth of the current supply:

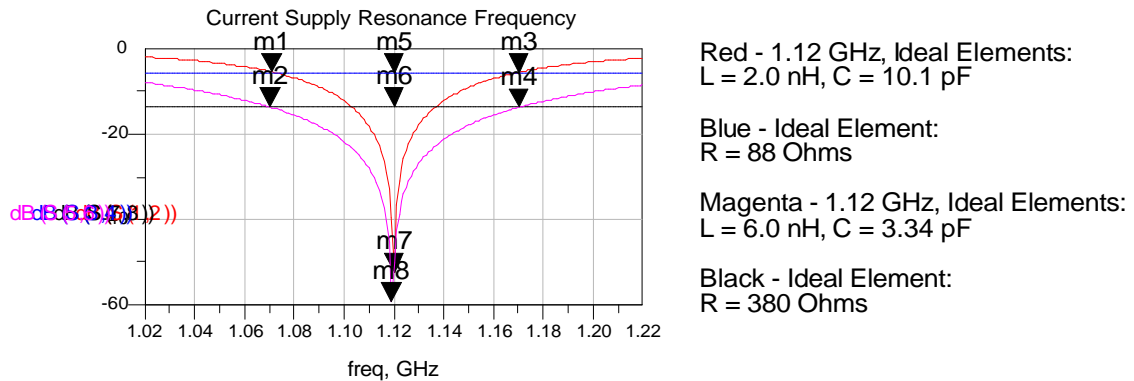
The parallel resonator current supply serves two functions. One, the inductor in the resonator has little voltage drop; parasitic resistance contributes approximately 32 mV at the 25 mA drain current of the new DFET VCO. Therefore the transistor drain is biased very near to the supply rail. Two, the parallel resonator appears to the transistor drain as a high impedance branch. So, the power of the oscillator will flow through the output port, not into the voltage supply. However, the resonator's high impedance is

frequency dependent. At the resonant frequency an ideal element circuit produces a very high impedance, yielding a transmission coefficient,  $S(2,1)$  through the resonator greater than -50 dB. However, the high impedance aspect of a parallel resonator is frequency dependant. The below circuit, setup for linear S-Parameter simulations will demonstrate how the high impedance of a parallel resonator diminished quickly as the operating frequency shifts away from the resonance frequency.

Current Supply Resonator Ideal Element Values



An ideal resistor is simulated simultaneously with the parallel resonator to provide an ohmic comparison to the transmission coefficient result expressed in decibels, dB. The simulations show a 5% shift away from the resonant frequency lowers the transmission coefficient from -52 to -5.5 dB. An 88 ohm series resistor produces -5.5 of attenuation, and 380 ohms produces to -13.6 dB. To produce -50 dB,  $R = \dots$



m1  
 freq=1.071GHz  
 dB(S(1,2))=-5.429

m3  
 freq=1.170GHz  
 dB(S(1,2))=-5.531

m5  
 freq=1.120GHz  
 dB(S(3,4))=-5.483

m7  
 freq=1.120GHz  
 dB(S(1,2))=-52.368

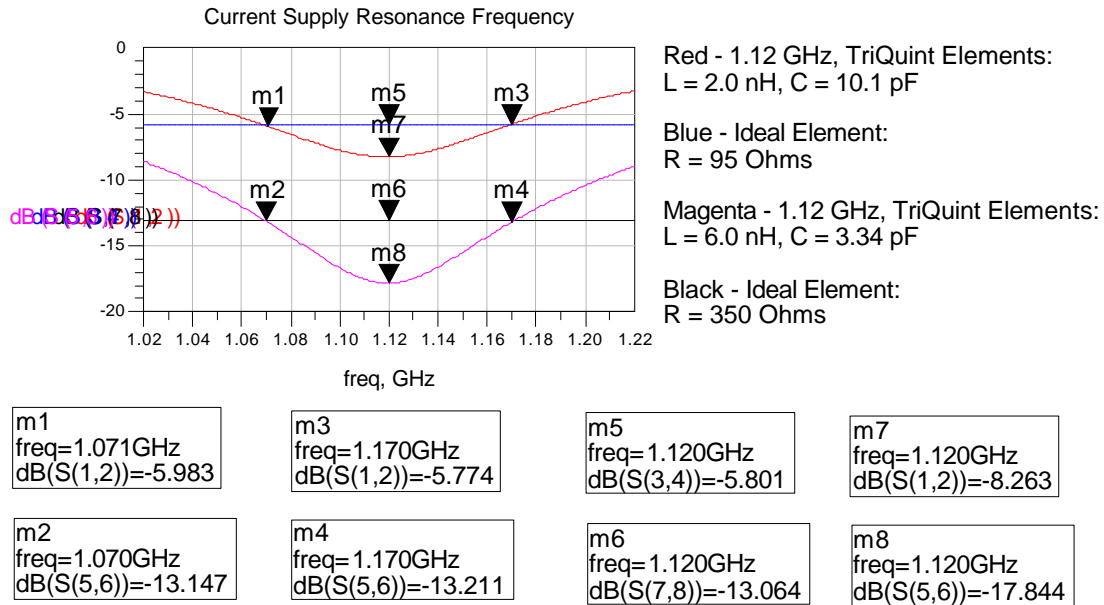
m2  
 freq=1.070GHz  
 dB(S(5,6))=-13.610

m4  
 freq=1.170GHz  
 dB(S(5,6))=-13.734

m6  
 freq=1.120GHz  
 dB(S(7,8))=-13.625

m8  
 freq=1.119GHz  
 dB(S(5,6))=-59.287

As shown in the previous graph, changing the resonator element values from  $L = 2.0 \text{ nH}$  and  $C = 10.1 \text{ pF}$  to  $L = 6.0 \text{ nH}$  and  $C = 3.37 \text{ pF}$  increase the impedance from approximately 88 to 380 ohms, for ideal elements. What kind of changes occurs with real elements? The largest discrete inductor in the ADS TriQuint palette is 6 nH. Rewriting the resonance equation in terms of  $C$  yields  $C = \frac{1}{(2\pi f)^2 L}$ . Solving for  $C$  yields  $C = 3.37 \text{ pF}$ . Substituting TriQuint elements into the resonator circuit, yields the below graph.



Although the very high impedance at the resonant frequency is lost, due to parasitic losses included in the TriQuint models, the bandwidth of the resonator's impedance improves from -5.8 dB to -13.2 dB, with the larger inductor.

Provide more circuit gain:

The gain in this oscillator circuit is the gain of the MESFET common source amplifier. The unilateral transducer power gain,  $GTU$ , is the most useful definition of gain for an amplifier because it takes into consideration the source and load mismatches<sup>6</sup>.

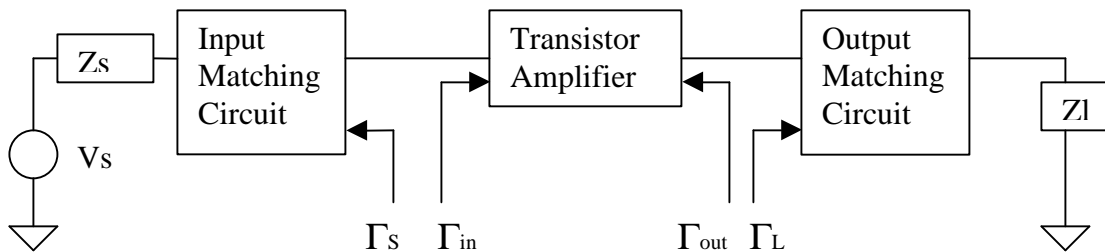
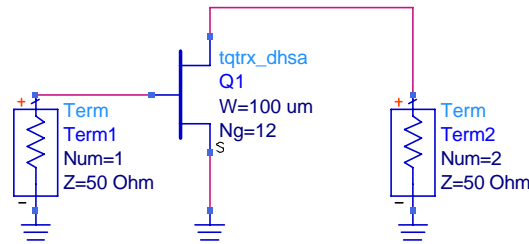


Figure 11.8, redrawn from Pozar, p.610.

As illustrated above, GTU is comprised of three components; the input matching circuit,  $G_S$ , the transistor,  $G_O$ , and the output matching circuit,  $G_L$ . Where:  $G_S = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2}$ ,

$$G_O = |S_{21}|^2, \text{ and } G_L = \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2}. \text{ However, as its name implies, these simplified GTU}$$

formulae are valid only if the transistor is a unilateral device,  $S_{12} = 0$ , or very small. To confirm that  $S_{12}$  is very small, examine the S parameter file of the device in question or simulate or test the device.  $|S_{12}| = 0.050$ , at 1.17 GHz, in the below S parameter simulation circuit. The GFET device value is 0.022; both values are close enough to zero to satisfy the simplification requirement, that the device is unilateral.



S parameter simulations of bare transistors yielded the following results.

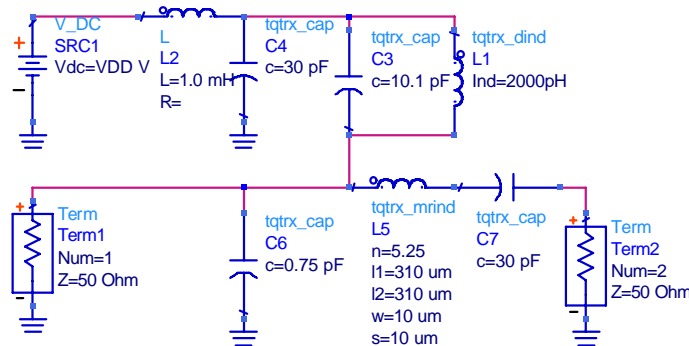
**Bare FETs**

DFET	S11	S21	S22	$\Gamma_L$	$\Gamma_S$	$G_S$	$G_O$	$G_I$	GTU
f_L	0.968	0.047	0.818	0.327	0.335	1.944327	0.002209	1.664386	0.007149
f_C	0.965	0.048	0.818	0.302	0.296	1.787901	0.002304	1.602943	0.006603
f_H	0.963	0.05	0.818	0.285	0.258	1.652622	0.0025	1.562304	0.006455

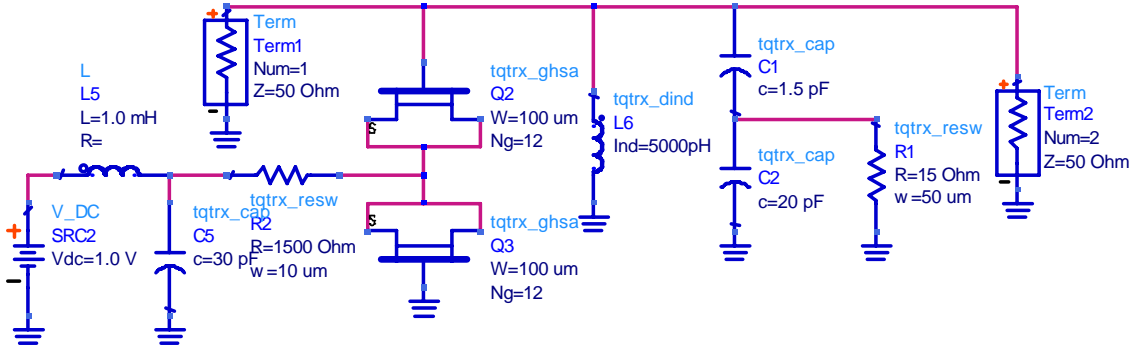
**GFET**

GFET	S11	S21	S22	$\Gamma_L$	$\Gamma_S$	$G_S$	$G_O$	$G_I$	GTU
f_L	0.983	0.021	0.863	0.209	0.122	1.271888	0.000441	1.423521	0.000798
f_C	0.981	0.022	0.863	0.074	0.093	1.20039	0.000484	1.134842	0.000659
f_H	0.98	0.022	0.863	0.15	0.068	1.142586	0.000484	1.289821	0.000713

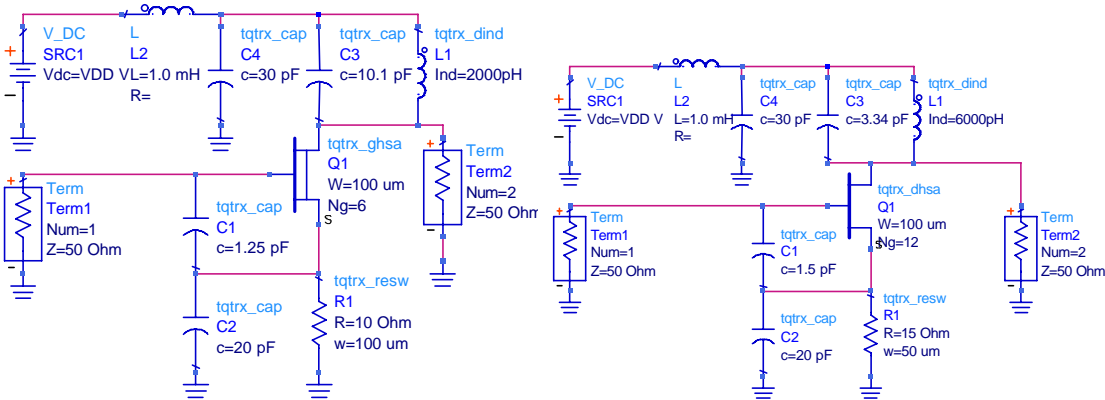
The above table calculates the GTU at the low, center and high frequency points in the specified range of operation. The OMN for bare device gain calculations is all the components forming a path to ground from the transistor gate, as shown below for the GFET device.



The IMN is similarly all the components on the input side, connected to the transistor gate, as shown below for the DFET device calculations.



The results table indicates the DFET amplifier has 10X the gain of the GFET amplifier. However, device manufactures provide S parameter data for devices under various biasing conditions. Therefore, perform the gain calculation for the devices under their respective biasing conditions. The two biased FET devices in their respective circuits are shown below.



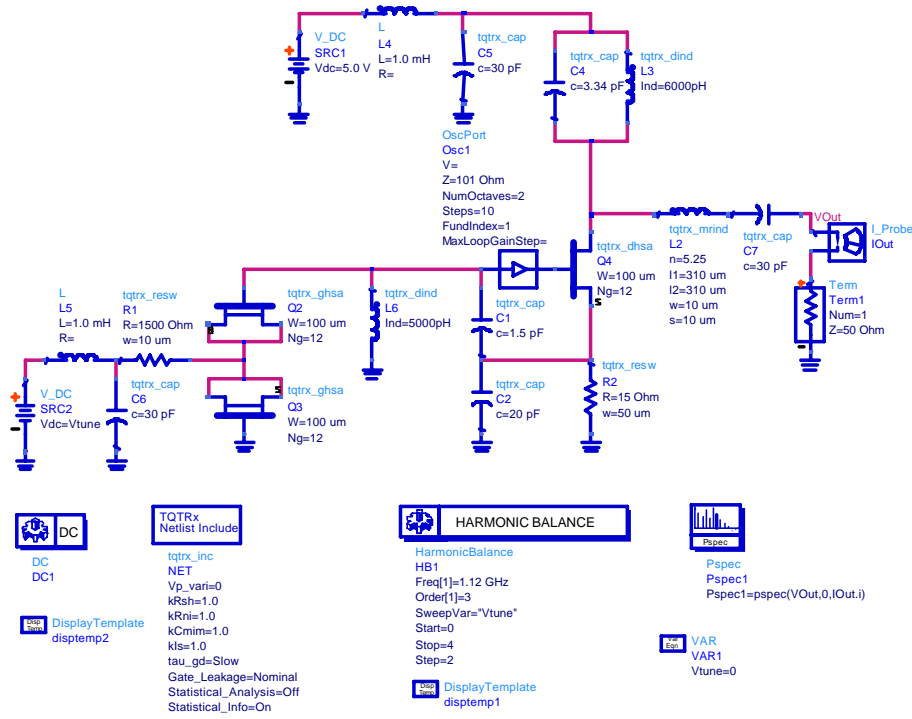
Gain calculations on bias FETs yield less disparity, yet the DFET circuit still has approximately three times the gain of the GFET circuit. And, better matching of the output could improve further the DFET advantage.

Biased FETs

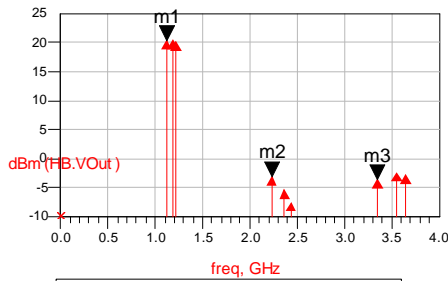
	S11	S21	S22	$\Gamma_L$	$\Gamma_S$	Gs	Go	GI	GTU
<b>DFET</b>									
f_L	1.391	5.524	0.583	0.339	0.292	2.594027	30.51458	1.374802	108.8233
f_C	1.34	5.316	0.611	0.356	0.271	2.284468	28.25986	1.426247	92.07669
f_H	1.297	5.092	0.633	0.373	0.252	2.066686	25.92846	1.475283	79.05449
<b>GFET</b>									
f_L	1.208	3.531	0.179	0.262	0.292	2.183398	12.46796	1.025267	27.91035
f_C	1.185	3.725	0.318	0.278	0.271	2.01051	13.87563	1.110359	30.97576
f_H	1.164	3.678	0.453	0.295	0.252	1.875297	13.52768	1.216346	30.85679

NEW 1.12 GHz VCO:

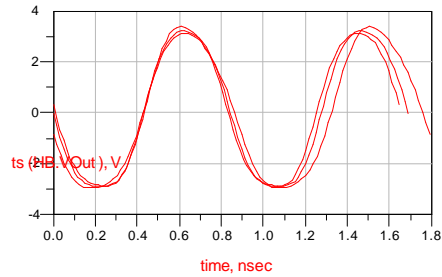
The redesigned 1.12 GHz VCO setup for a harmonic balance simulation.



Below are results from harmonic balance simulation on a circuit with no interconnects.



m1	freq= 1.115GHz
	plot_vs(dBm(HB.VOut), freq)=20.360
	Vtune=0.000000
m2	freq= 2.230GHz
	plot_vs(dBm(HB.VOut), freq)=-3.082
	Vtune=0.000000
m3	freq= 3.345GHz
	plot_vs(dBm(HB.VOut), freq)=-3.594
	Vtune=0.000000

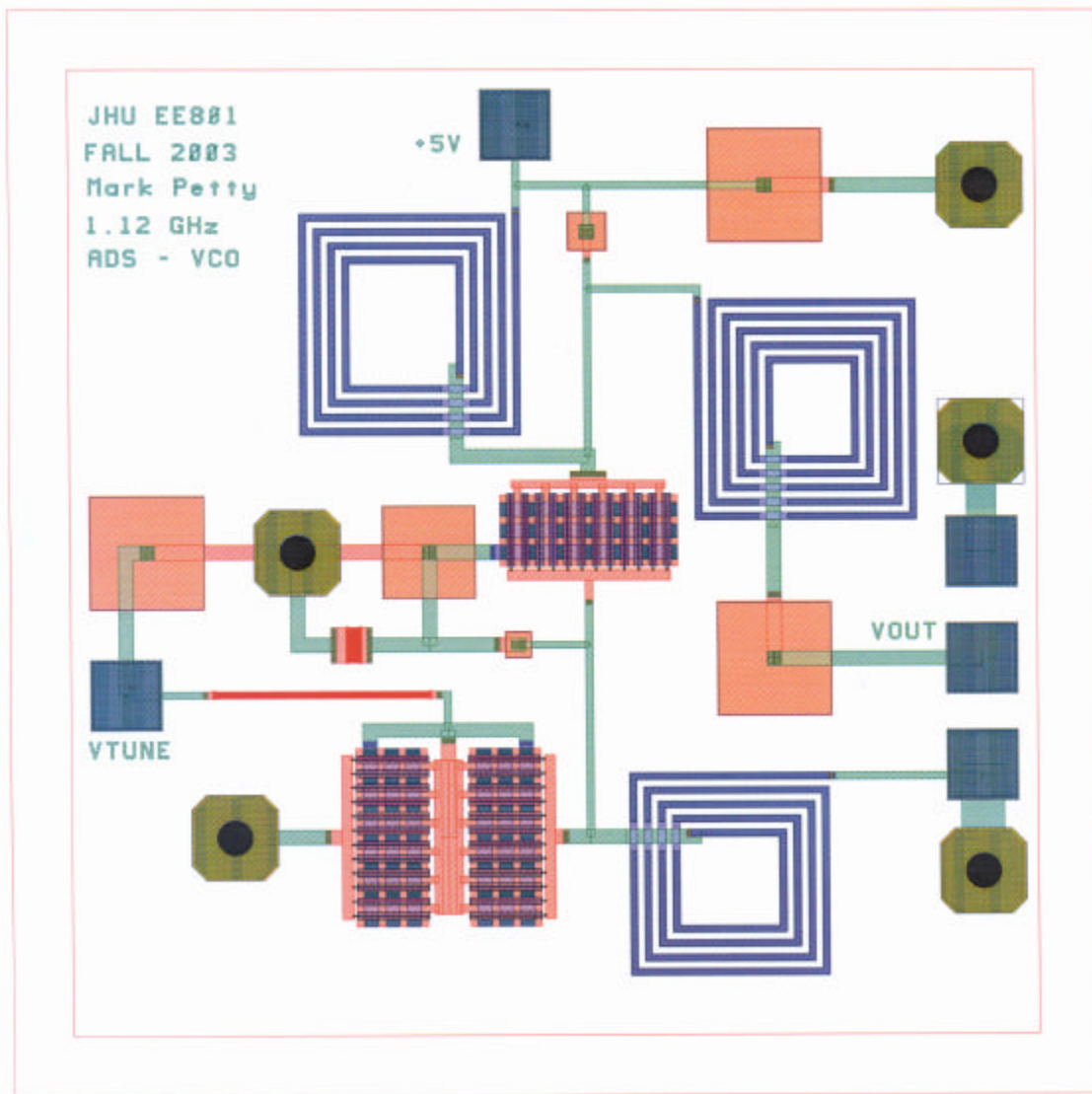


Eqn period = cross(ts(HB.VOut),1)  
Eqn frequency = 1/period

time	period	frequency
Vtune=0.000	426.8psec	0.0000 sec
	1.324nsec	896.9psec
		1.115E9
Vtune=2.000	431.3psec	0.0000 sec
	1.277nsec	845.6psec
		1.183E9
Vtune=4.000	429.8psec	0.0000 sec
	1.253nsec	823.0psec
		1.215E9

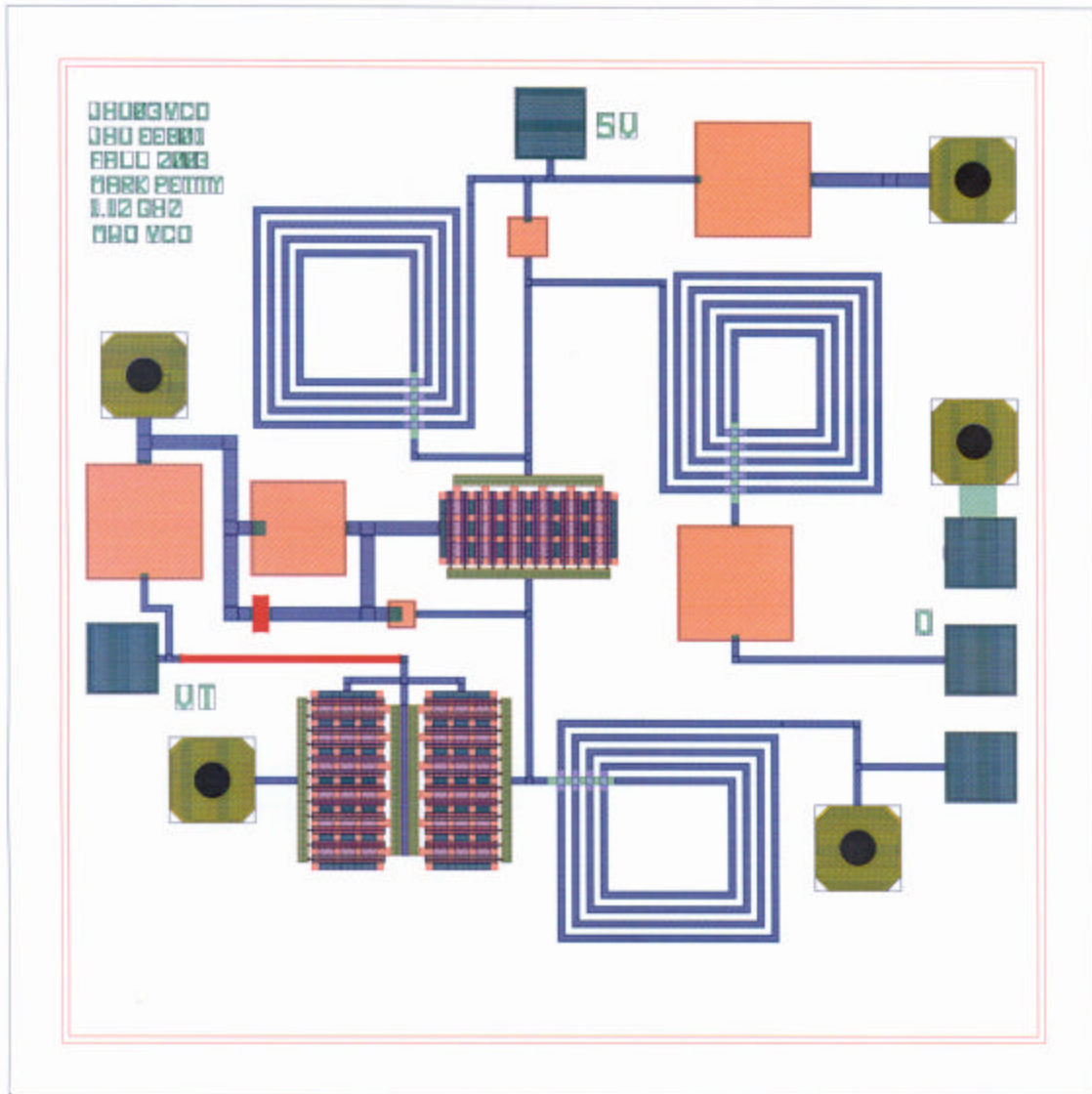
The previous device, when fabricated, had an output frequency approximately 50 MHz below the design simulations. Therefore, the output frequency of this circuit was purposefully designed approximately 50 MHz high.

The VCO design fits easily onto the ANACHIP frame, as shown below.



## Microwave Office Comparison:

One of the original intents of this project was to compare simulation results from both Applied Wave Research's Microwave Office, MWO, and Agilent's ADS tool to measured data from a fabricated chip. However, later than expected delivery of the software and problems executing the TriQuint process library file limited the MWO aspect of this report to the layout of a nearly identical 1.12 GHz VCO, with the idea that simulations on the design would be completed later.



### *Conclusions:*

The common source configuration for MMIC VCO design is problematic. The output frequency is unpredictable without EDA tools. The output frequency is affected by not only the input resonator tank, but both the external gate to source capacitance and the output matching network. Following the design methodology in the gEE-CAD tutorial, the resultant circuit had a gate transmission line of  $\sim 2700 \mu\text{m}$  and a drain transmission line length of  $\sim 7000 \mu\text{m}$ . And then both the harmonic balance and transient simulations failed to oscillate. Although this circuit configuration can yield a clean sinusoidal output, a repeatable design methodology that could predict the output frequency without excessive tweaking of element values was not found. Therefore, the author does not recommend using a common source configured VCOs.

The author would like to thank the Agilent Technologies, for the license to use their ADS software at home, and Gary Wray, their technical consultant whom jovially guides the class through many fits and starts during the semester. Thanks also to John Penn and Craig Moore, for their guidance and understanding through this troubling semester.

To Mr. Moore and Mr. Penn, this design may be over, but the project continues...

### *REFERENCES:*

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6. D. Pozar, *Microwave Engineering*, 2<sup>nd</sup> ed., New York, J. Wiley & Sons, p. 610.