The Johns Hopkins University

Applied Physics Laboratory

Microwave Monolithic Integrated Circuit Design

Class # 525.787

Final Project: S-band VCO

By

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Abstract:

This paper describes the design of an S-band voltage controlled oscillator, VCO. The VCO is one of nine MMIC designs that make up an S-band transceiver. The design tool used for this project was Advanced Design System, ADS. The VCO's target of fabrication is TriQuint Semiconductor's Texas 0.6µm Gallium Arsenide fab. The target parameters for the S-band controlled oscillator include: a center frequency of 2762 MHz; a tuning range of +/- 50 MHz; minimum output power of +10dBm, desired output power of 13dBm; supply voltage of +/- 5 volts, desired supply voltage of +5 volts only, tuning voltage of 0-5 volts; output impedance 50 ohms, nominal; and sized to fit on the 60 X 60 mil TriQuint ANACHIP.

Introduction

A simplex MMIC transceiver implemented in the Triquint TQTRx process (4 mil thick GaAs) with simulation and layout in Agilent ADS has been designed for C-Band HyperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequency applications.

The system utilizes a C-Band Up-Down Converter with a 275MHz intermediate frequency (IF) that can be down-converted to baseband with a second 275MHz local oscillator (LO). The second LO is upconverted to the C-Band in TX mode and modulation can be introduced onto the second LO or through direct frequency modulation of the VCO in the transceiver. The dual band usage VCO with high side (HSLO/LSLO) injection to the mixer is specified for operation from 2712MHz to 2813MHz, which when doubled is between the WLAN and ISM frequencies.

Receive and transmit signals are routed by C-Band single-pole-double-throw (SPDT) switches. The receive chain consists of a cascaded low noise amplifier (LNA) and post amplifier. The transmit path employs a variable gain amplifier for level control and a driver amplifier preceding a 0.25 Watt power amplifier.

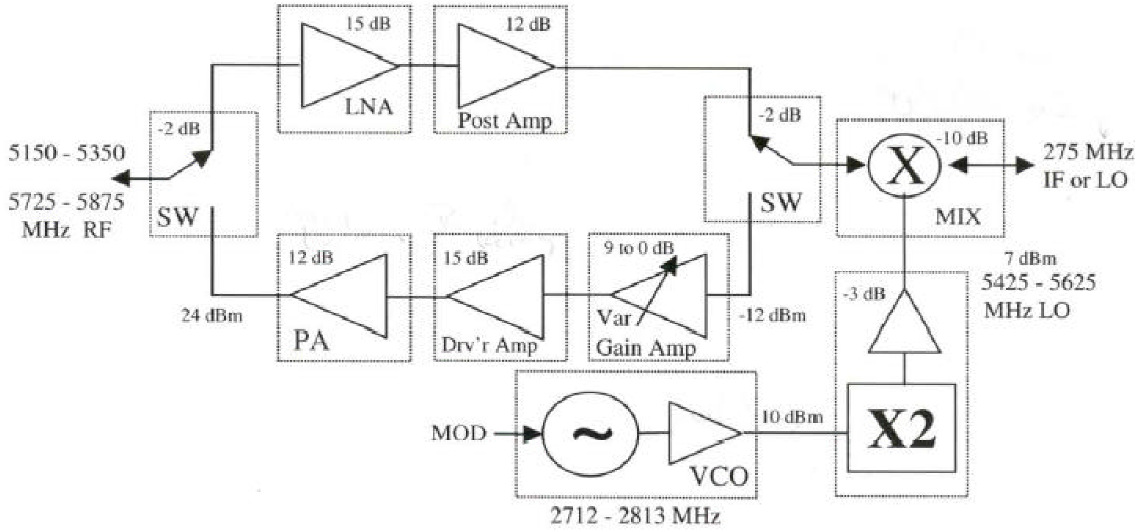


Figure 1. Chip-Set for the 5150 – 5350 MHz WLAN and 5725 – 5875 MHz ISM Bands.

Design Philosophy

The VCO architecture is based upon small negative impedance theory where the active circuit is represented by the impedance,

$$Z_a=R_a+jX_a$$

It can therefore be observed that

$$Z_l=R_l+jX_l$$

As shown in Fig. 3. Assuming that a steady state oscillation is occurring between the two networks then there must exist a loop current, I, that is non-zero. Using Kirchoff's law, the total loop voltage then must be zero which yields

$$Z_a + Z_l = 0.$$

It can therefore be observed that

$$Z_{a} = - Z_{l} \text{ (negative impedance)}$$

to ensure oscillation and hence the nomenclature of the theory and design technique.

Furthermore, in small signal design, the imaginary portion of this relation is of particular interest and thus

$$X_a + X_l = 0$$

The large signal operation of the FET oscillator can then be predicted from its small signal characteristics since as the signal grows to steady state, the actual change of the imaginary portion of the active circuit is small.

The differential change in the active circuit impedance versus the operating point amplitude and frequency delta variations as described by Kurokawa is then,

$$[dR_a/dA][dX_1/d\omega] - [dR_1/d\omega][dX_a/dA] > 0$$

Where R_a is the active device’s negative resistance, A is the steady state amplitude, and ? is the frequency. As stated earlier, the change in X_a with respect to amplitude is small and considered to be zero. However, for GaAs FET oscillators, R_a increases positively with respect to amplitude since the negative resistance of the circuit decreases in magnitude with increasing amplitude. Therefore applying these conditions, then

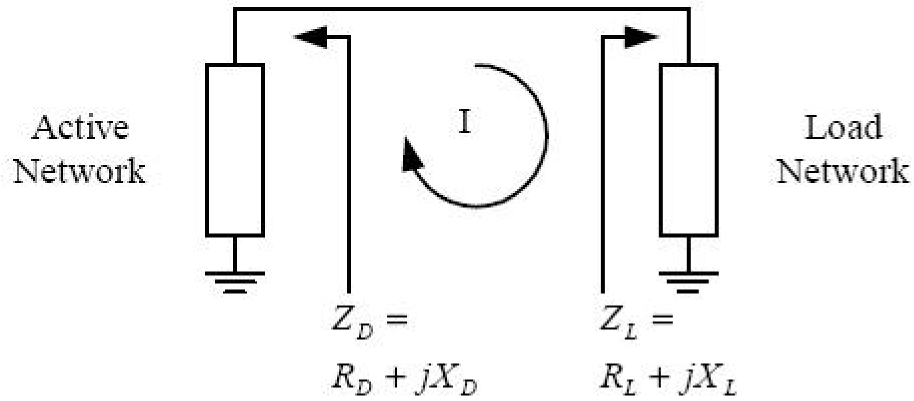
$$[dX_1/d\omega]_{\omega 0} > 0$$

which implies that stable oscillations are ensured when the reactive component of the load impedance has a positive slope versus frequency, and the frequency of the oscillation corresponds to the zero crossing of the frequency axis.

Additionally, it has been shown that for a series resonant oscillator that

$$|R_a| \sim\geq 3R_1$$

to approximate a power impedance match between the load circuit and the large signal steady state oscillations. The factor of 3 is itself a compromise based upon the experimental trade-off between start-up conditions and final oscillation frequency.



Design description

The VCO is powered by a 5 volt power supply. The 0 to -5 Volt voltage controlled oscillator operates from 2712-2813MHz with output power of 11.6 dBm. The VCO features a, W=100µm, N=6, TQTRx_GFET and was biased at the drain with 2 inductors for RF blocking. To destabilize the FET, we connect the FET to a series resistor to ground. Series source resistor provides a feedback path from drain current to gate voltage. To get MAXMP2 to be approximately 3, we adjust the source resistor. This feedback increases mainly the magnitude of the S_{12} parameter making the circuit more unstable (figure 1.1).

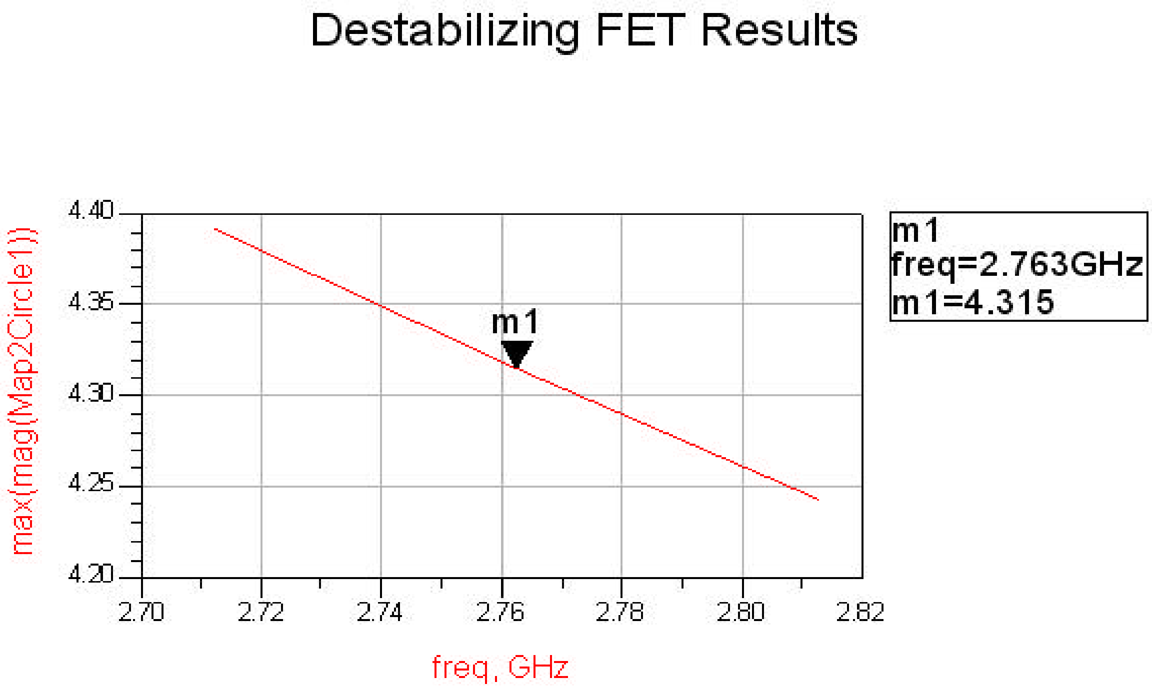


Figure 1.1

Now that the FET has been de-stabilized, the next step is to develop the necessary impedance for the active network. This was achieved by adding the input matching network which contained a varactor diode and lumped elements. The lumped elements were tuned such that the overall impedance of the active network has a negative real and imaginary part. This is illustrated in the figure below. Once the negative impedance of the active network is obtained, the next step is to develop the load network such that its impedance is the negative of the active network. This was obtained by first adding an inductor to the active network. The inductor was then tweaked such that the S_{11} and Z_{11} are totally resistive.

Schematic Prior to ¼ wave transformer

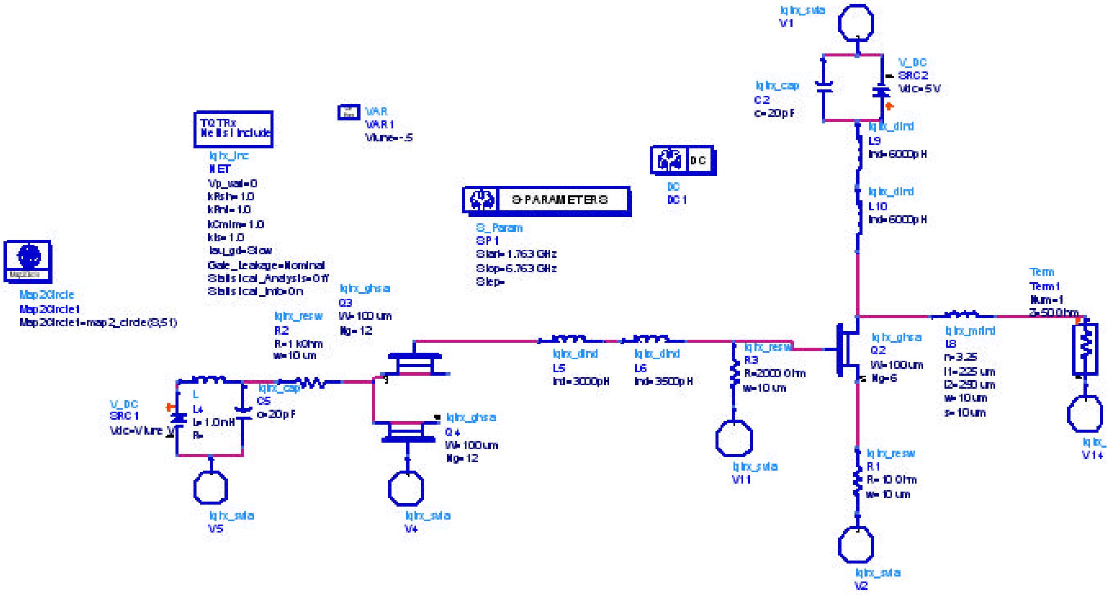


Figure 1.2

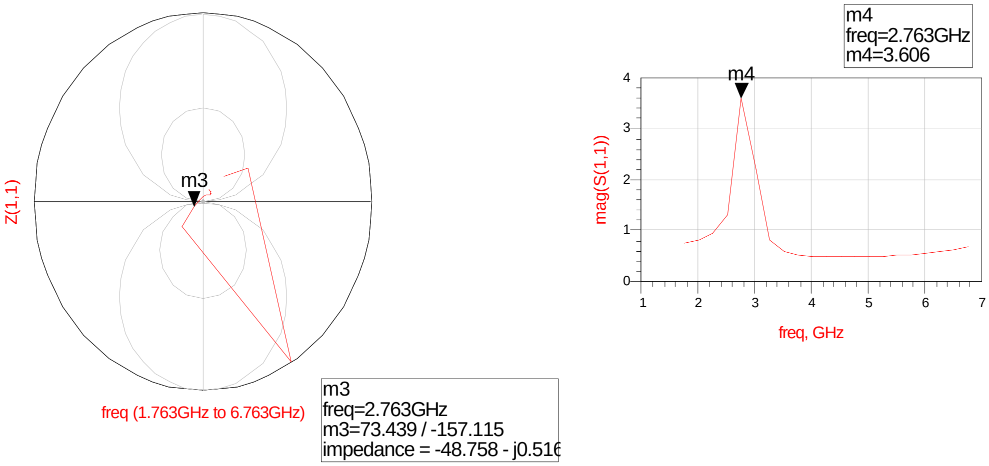


Figure 1.3

Once the reactive impedance of the active component was negated the next step was to transform the real impedance of the active network. This was achieved by using a ¼ wave transformer. The figure below shows how the start-up conditions was obtained comparing the impedance of the active network to the inductor and ¼ wave transformer.

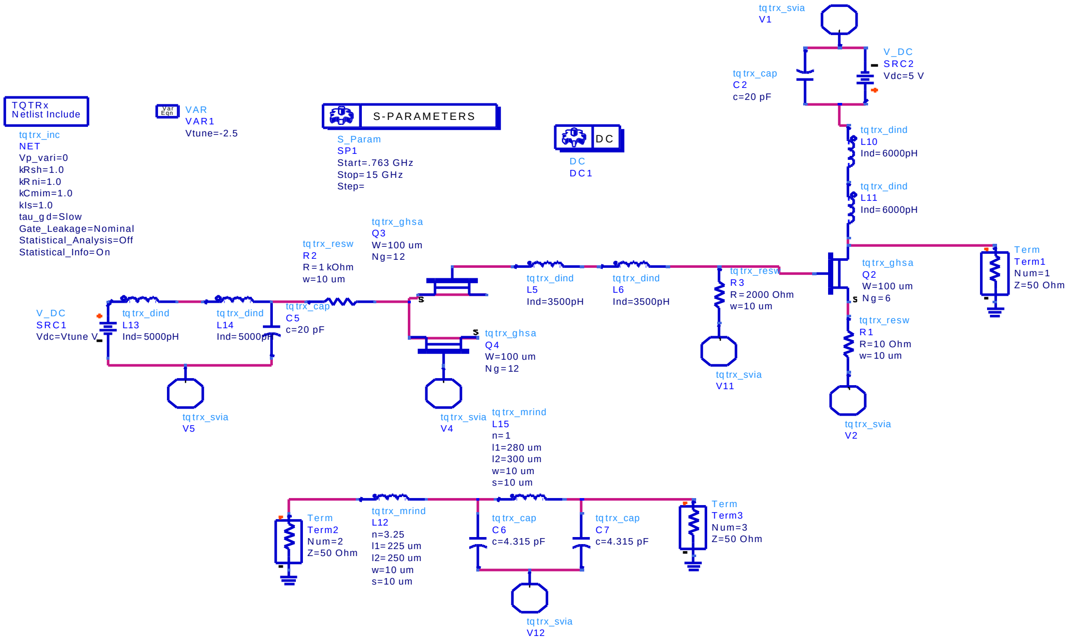
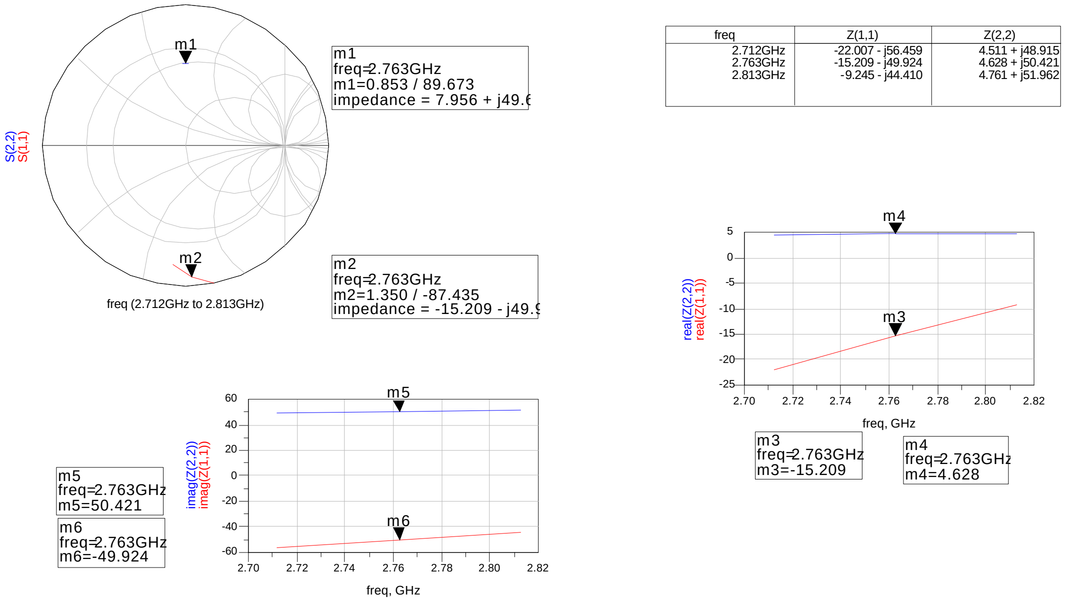
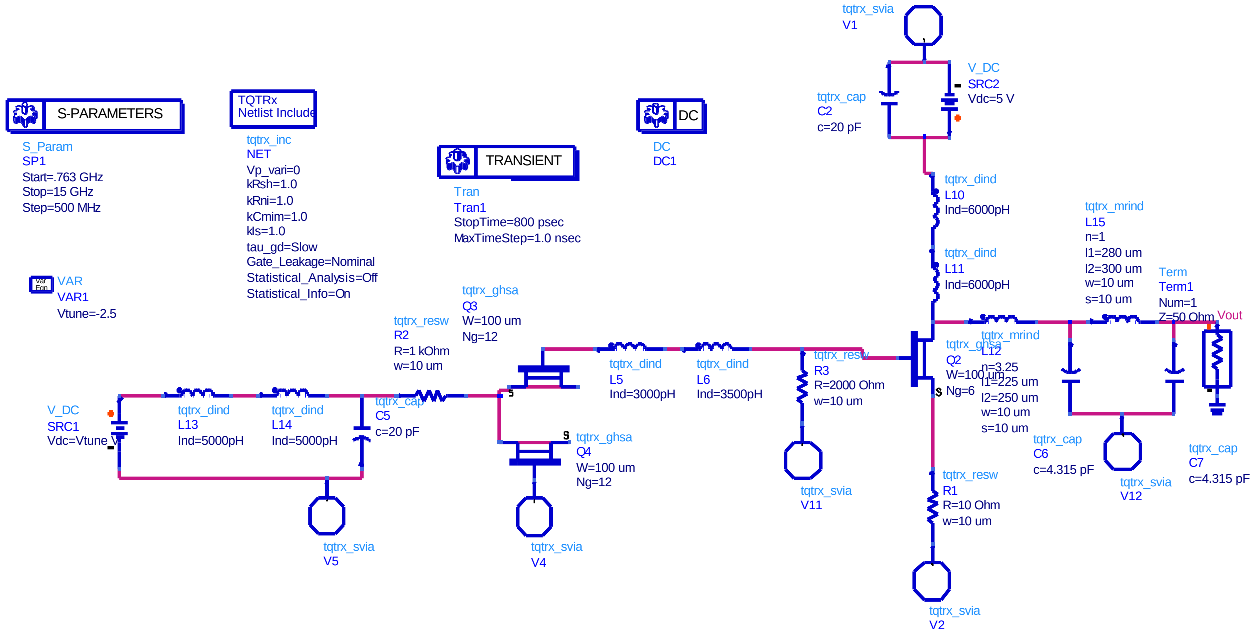


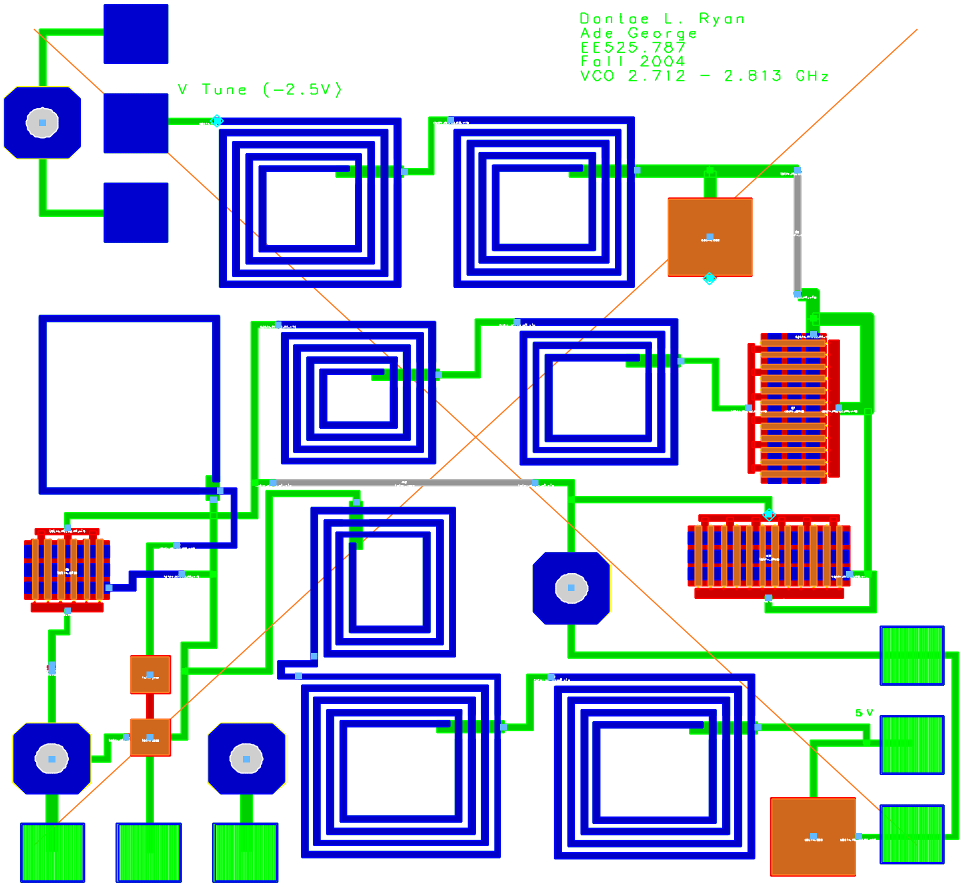
Figure 1.4



freq	Z(1,1)	Z(2,2)
2.712GHz	-22.007 - j56.459	4.511 + j48.915
2.763GHz	-15.209 - j49.924	4.628 + j50.421
2.813GHz	-9.245 - j44.410	4.761 + j51.962

Figure 1.5


S-PARAMETERS
S_Param
SP1
Start=.763 GHz
Stop=15 GHz
Step=500 MHz
TQTRx
Netlist Include
tqtrx_inc
NET
Vp_vari=0
kRsh=1.0
kRni=1.0
kCmim=1.0
kls=1.0
tau_gd=Slow
Gate_Leakage=Nominal
Statistical_Analysis=Off
Statistical_Info=On
TRANSIENT
Tran
Tran1
StopTime=800 psec
MaxTimeStep=1.0 nsec
DC
DC
DC1
VAR
VAR1
Vtune=-2.5
tqtrx_svia
V1
V_DC
SRC2
Vdc=5 V
tqtrx_cap
C2
c=20 pF
tqtrx_dind
L10
Ind=6000pH
tqtrx_dind
L11
Ind=6000pH
tqtrx_mrind
L15
n=1
l1=280 um
l2=300 um
w=10 um
s=10 um
Term
Term1
Num=1
Z=50 Ohm
Vout
tqtrx_ghsa
Q3
W=100 um
Ng=12
tqtrx_resw
R2
R=1 kOhm
w=10 um
tqtrx_dind
L5
Ind=3000pH
tqtrx_dind
L6
Ind=3500pH
tqtrx_resw
R3
R=2000 Ohm
w=10 um
tqtrx_ghsa
Q2
W=100 um
Ng=6
tqtrx_mrind
L12
n=3.25
l1=225 um
l2=250 um
w=10 um
s=10 um
tqtrx_cap
C6
c=4.315 pF
tqtrx_svia
V12
tqtrx_cap
C7
c=4.315 pF
V_DC
SRC1
Vdc=Vtune V
tqtrx_dind
L13
Ind=5000pH
tqtrx_dind
L14
Ind=5000pH
tqtrx_cap
C5
c=20 pF
tqtrx_ghsa
Q4
W=100 um
Ng=12
tqtrx_svia
V11
tqtrx_resw
R1
R=10 Ohm
w=10 um
tqtrx_svia
V5
tqtrx_svia
V4
tqtrx_svia
V2



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