

# **An Active Cascode Mixer With Inter-stage Matching**

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in Engineering and Applied Science.  
EE787 Fall 2003

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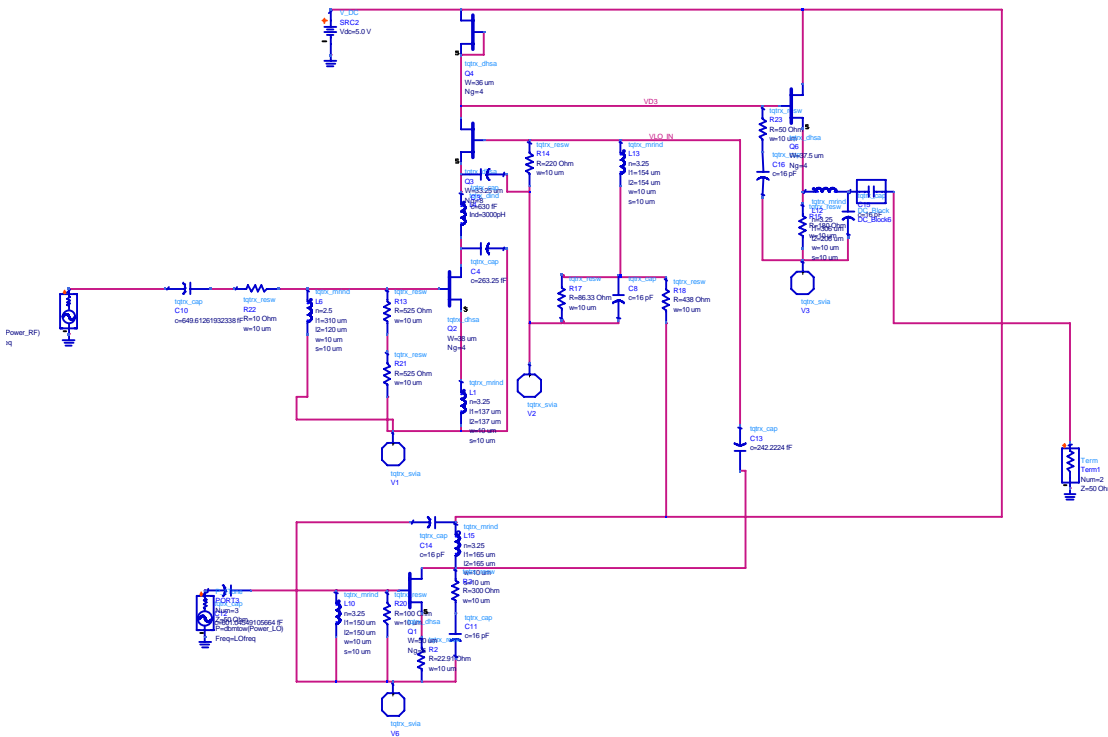
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## 1. Abstract

The following paper presents a 5.8GHz active, down converting, mixer; producing an intermediate frequency (IF) of .5-20MHz. The circuit is a variant of the dual gate mixer. It uses two separate MESFETs and inter-stage matching to maximizing the conversion gain while maintaining the

desirable isolation characteristics of the dual gate mixer. An on-chip amplifier for the local oscillator is integrated with the circuit. The entire circuit is biased using a single +5V supply, drawing approximately 250mW of DC power. The mixer and the amplifier for the local oscillator are all successfully laid out on a 60mil by 60mil chip using the Triquint TQTRX process.

RF Schematic Figure 1,



## 2. Circuit description

The circuit can be divided into three sections the mixer the LO amplifier and the IF buffer. The mixer can be further subdivided into the RF common source amplifier stage and the LO common drain stage. Each of these sections provides a distinct function and will be addressed separately.

The core of the design is the mixer itself. The mixer topology is based on the traditional dual gate mixer. In the dual gate

mixer a FET with two gates is employed with the upper most gate being driven by the LO and the lower gate being driven by the RF. The mixing would take place as a result of the nonlinear characteristics of the IV curves of the two channels. The dual gate mixer is often modeled as a stack of two distinct FETs in a cascode arrangement. The mixer design presented here takes this model literally. Two distinct FETs are used in the cascode arrangement with inter-stage matching (See figure 1) to maximize the gain and power transfer between the LO and

the RF signals in the hopes of achieving significant conversion gains while maintaining the isolation benefit of the dual gate topology.

As in the dual gate mixer the lower FET is driven by the RF input signal. This FET looks like a common source amplifier and was designed as such (See figure 2) with the notable exception that the bias point is chosen at the edge of the saturation region to facilitate mixing when this FET is presented with the LO at the drain. In this case the matching criteria was simply to get reasonable gain. As such a simultaneous available gain match of 8 dB was the design target. (see figure 3) A source inductor and a shunt resistor at the gate, both had to be used to stabilize the amp. The input match is implemented by way of a series capacitor and a shunt inductor. This matching network provides DC blocking, and an easy access point for the DC bias to the gate at the expense of some bandwidth. Two element matches were chosen exclusively throughout the circuit due to space constraints with similar trades offs between space and bandwidth. The output matching circuit consisted of a series inductor and a shunt capacitor; which is the only feasible arrangement that will not interfere with the DC bias.

Figure 2. RF Input Schematic

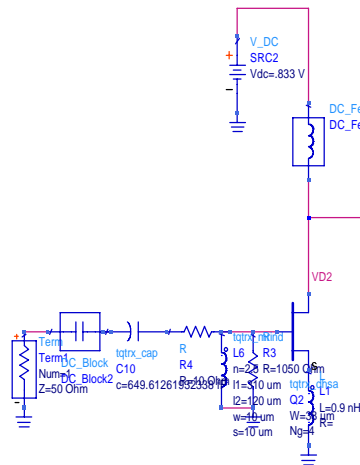
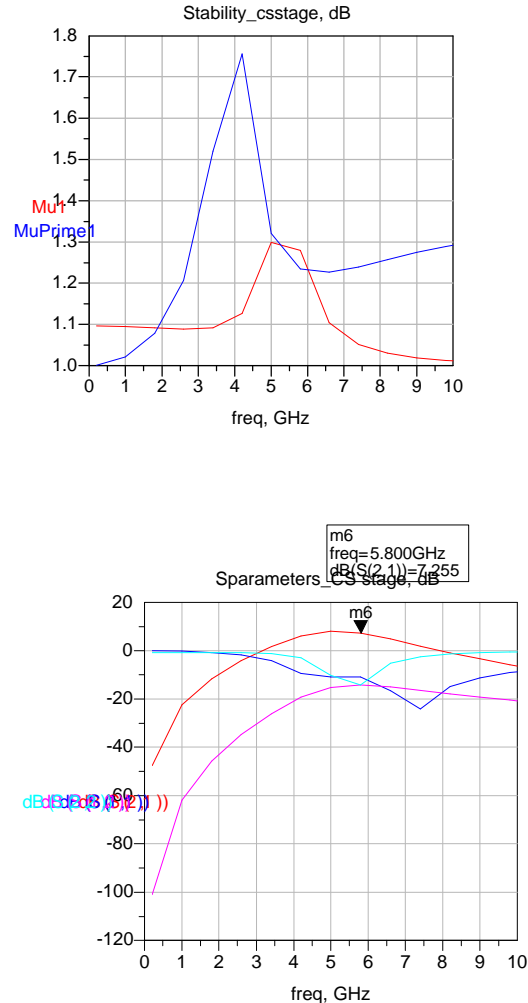


Figure 3 Spams and stability for RF input stage



The second aspect of the mixer is the upper FET, which is driven by the amplified local oscillator (LO). The upper FET can look like any of the three basic amplifier types depending on the perspective considered. To the LO it looks like both a common drain and common source amplifier. The output of the lower FET is appears as either the output of a common drain stage or the input to a common gate stage. And to the IF port it appears as the output of either a common source or common gate amplifier. To varying degrees the upper FET acts as all

these things. The function that is most critical to our purpose is the common drain amplifier (See figure 4), because this will present the LO signal to the lower FET to facilitate mixing. Thus this matching of this circuit was designed with the idea of limiting the loss in the follower to less than 3 dB. (see figure 5) The output matching network was designed as a shunt capacitor and a series inductor as in the lower FETs output stage so as not to interfere with the DC bias of the mixer. A shunt resistor was place at the gate to aid with stability and the DC bias is provided by a resistor network that also serves to make the input to the FET appear close to 50 ohms. Upon simulating the characteristics of the input of the upper FET it was found that the input to the FET was sufficiently close to 50 ohms that an additional reactive matching network was not warranted when weighed against the space it would require.

Figure 4 Common drain LO Input.

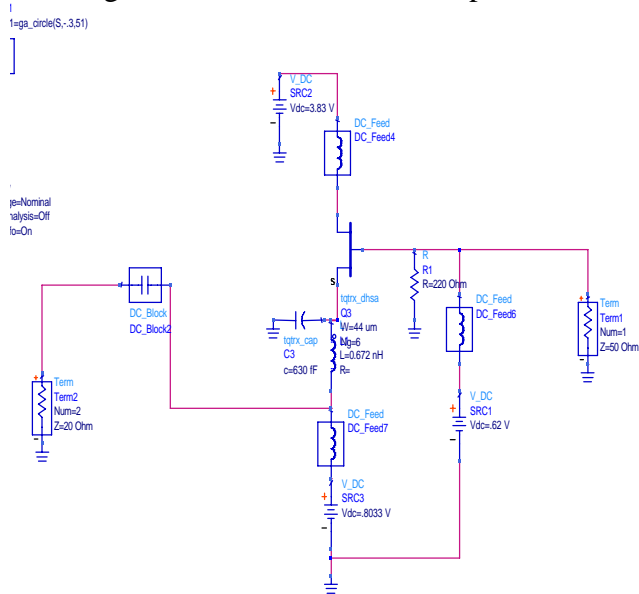
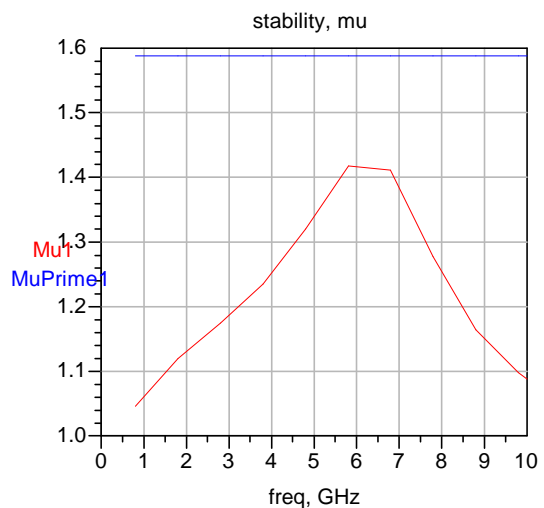
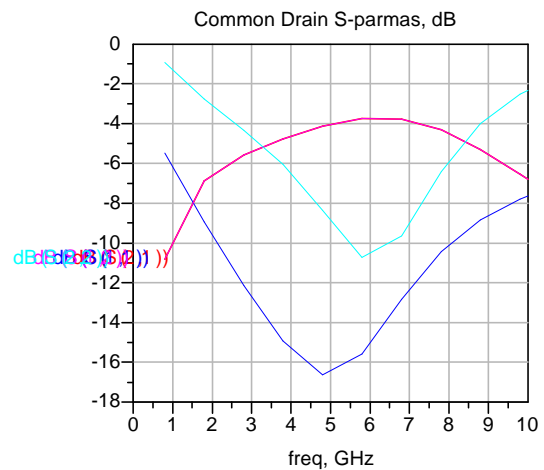


Figure 5, LO Common Drain stage Sparams and stability



The effects of the other amplifier effects were only considered in terms of their effect on stability. The common gate stage presented to both the IF and RF signals could be beneficial in attaining conversion gain but it was not pursued in this design. The common gate and common source behaviors do present a concern for stability and as such a series resistor on the input to the lower FET and a shunt resistor on the IF port were added after the sections were combined to correct an observed stability concern.

Once the mixing takes place the IF signal, along with the RF and LO is presented at the drain of the upper FET. As the IF is .5 - 20MHz in this design Low frequency circuit concepts are easier to consider and just as applicable as RF concepts. The drain of the upper FET experiences significant loss in the IF signal when presented with a 50ohm load. The gain improves as the load resistance increases. This is a classic low frequency current drive problem and is easily addressed by adding a follower stage to the output. No input matching is needed or desired as the large, at < 20 MHz, gate impedance of the FET is the desired. The final functional portion of the circuit is the LO amplifier. This is a simple common drain amplifier (see figure 6) added to gain up the LO to provide a larger LO signal to the gate of the upper FET. The only design consideration here is that the gain not be overly large, as there is a direct tradeoff between LO gain and LO to RF isolation. A gain of 7 was the design target and once again a series capacitor and shunt inductor provided the input matching to facilitate DC blocking and applying the DC bias to the gate. On the output side a shunt resistor capacitively linked to ground is added to aid stability and as always the series capacitor and shunt inductor matching network was used.

apparent load. Passive matching on the output of the follower was not feasible due to the large physical size of components to match at < 20MHz. Filtering was opted for instead of matching as component size to effectively filter the LO and RF was much more reasonable. It is possible to match the IF by having appropriately sizes FETS in the follower stage but this was neglected due to time constraints; under the assumption that, at the IF frequency, the gains of power matching are minimal when confronted with the utility of using low frequency circuit techniques once the RF has been down converted.

Overall the various components integrated very well in simulation. The stability problem mentioned earlier was the only difficulty noted in the integration phase.

Figure 6 LO amplifier

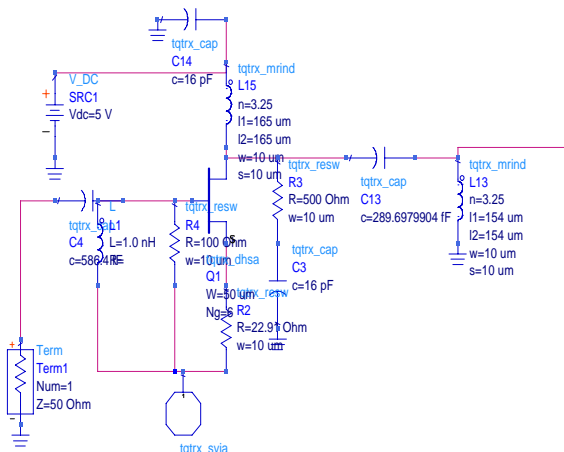
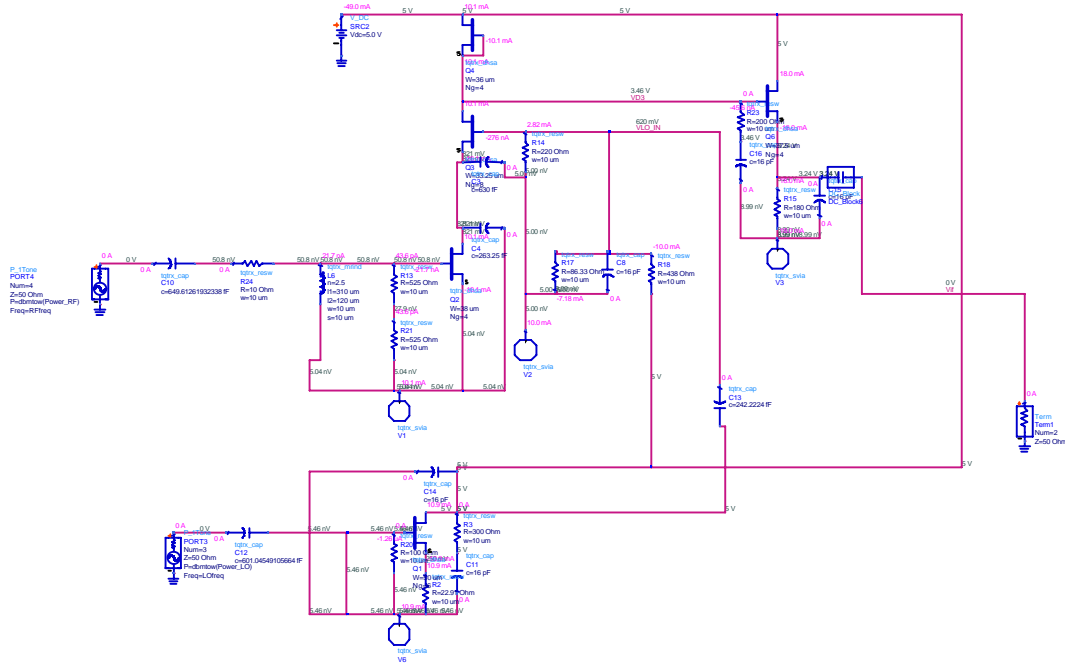


Figure 7 DC schematic.



### 3. DC Bias Description

The DC biasing of this circuit deserves some special attention. Care must be taken with the biasing of the cascode mixer section as one must bias a stack of FETs as opposed to a single device. The biasing is achieved by using an appropriately sized FET biased as an IDSS current source applying 10mA. (see figure 7) The controlled current is used to force the FETs to a certain VDS as opposed to the more common method of a controlled point on the IV curve and, at DC, acts like a source resistor relative to the upper FET. So, the upper FET is sized to pass slightly more current than the current source provides at a VDS small enough so as not to cutoff the current source above it (see figure 9). The gate bias generated by a resistive voltage divider but must be calculated relative to the VDS of the lower FET. It is significant to note that one must account for the stabilizing

VDS forcing the FETs to a specific current. This current is fed through the upper FET and in to the lower FET that is also biased at 0Vgs and is slightly larger, so that the Vds bias will fall at the knee between the saturation and triode regions of the IV curve (see figure 8) where maximum nonlinearity occurs and the most mixing can take place. The upper FET is now biased in a modified self-bias configuration. The controlled current being forced into the lower FET pulls the VDS of the lower FET to a specific resistor when calculating for the bias network.

Figure 8 Lower FET Bias point.

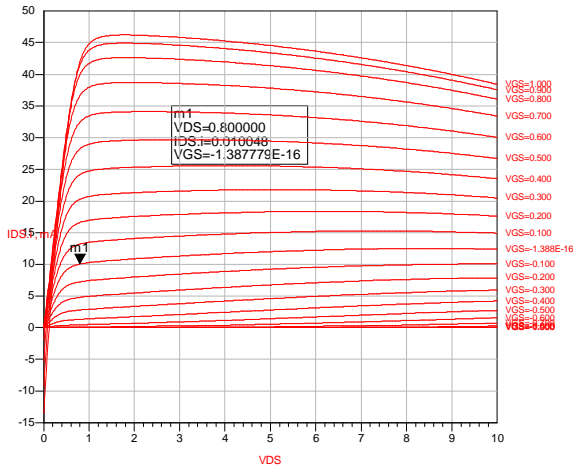
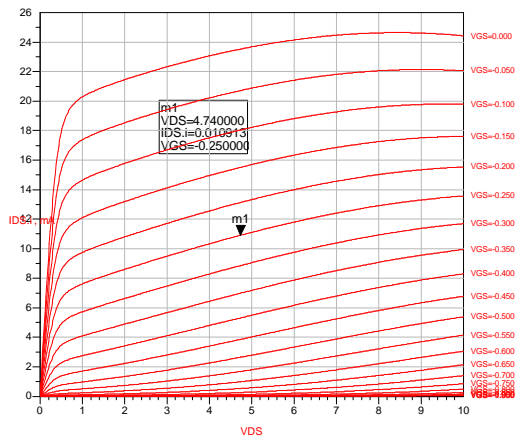


Figure 9 Upper FET bias point



The biasing of the other portions of the circuit is less involved. The follower is biased by selecting a desired current, in this case 20mA and appropriately sizing a FET for that current and providing a source resistor of a value sufficient to create the proper voltage conditions knowing that the gate voltage is the DC voltage at the drain of the upper FET of the mixer. The LO amplifier uses gate voltage of 0V and a FET appropriately sized to source 10mA

The results are shown in the following table and plots.

configured in the classic self-bias arrangement. (see figures 6)

The Circuit Layout is shown in figure 22. Bypass caps were placed at various points on the DC 5V line and 10um lines were the standard connection between elements. The only place where current capacity was a concern was in the follower load resistor which was increased to 40um in width to accommodate the 30mA bias current for this stage. There is some concern about the use of metal one in the connection to the FETs. However, this is a part of the standard library and is beyond my control.

#### 4. Simulation Results

The graphs below detail the relevant results. The three port S-parameters show isolation, matching and the various gains. (figure 10) The stability plots (figures 11-13) are of questionable accuracy since I am not certain that looking at a three port network in this fashion is valid and that it completely characterizes the inter-stage stability but the unconditional stability shown in these plots does provide reassurance that some basic stability criteria are met. As an aside stability simulations were done on internal nodes using high impedance terminations. The accuracy here is also questionable but these did indicate a stability problem at an internal node and in the interest of caution this problem was corrected as noted earlier. The VSWR (figure 17) is adequate and with a little additional work it appears that reasonable bandwidth is achievable. Lastly one can see the IF spectrum that shows the mixing products and the conversion gain (figure 18). The significant gain is in keeping with the design goal of gain while maintaining isolation.

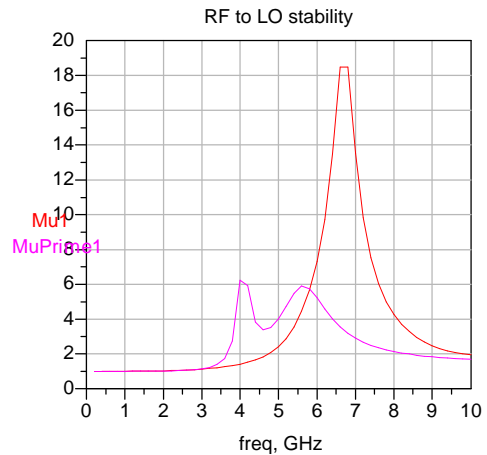
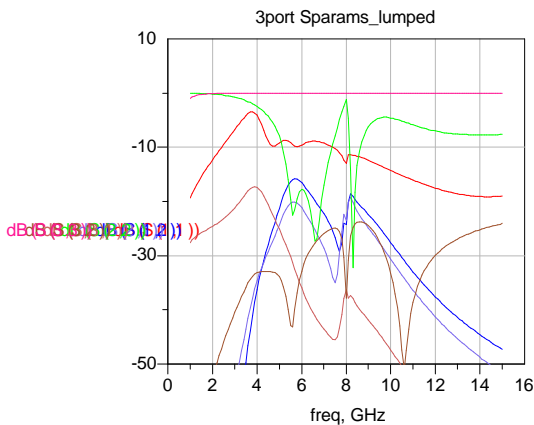
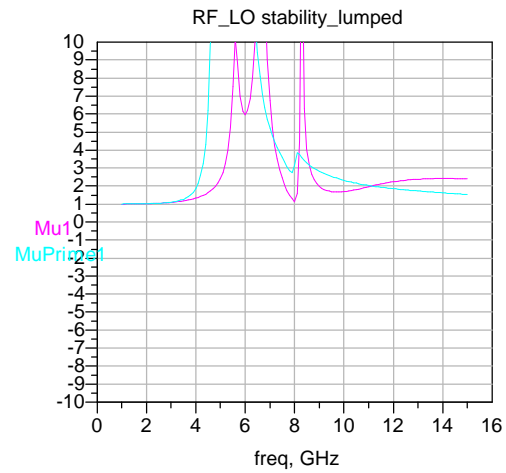
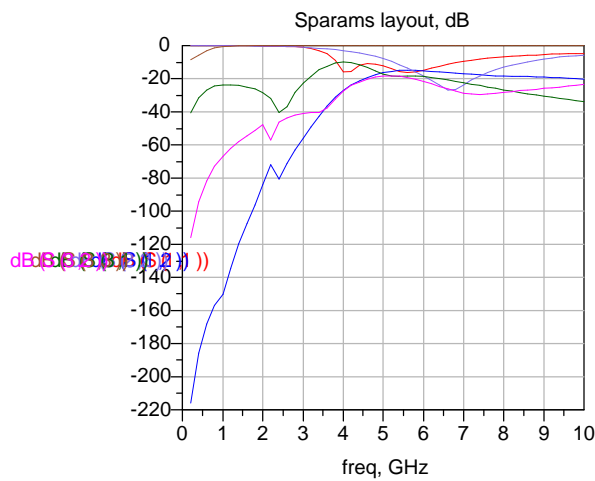
Specification Name	Conditions*	Specification requirement	Lumped Element Simulation	Layout Simulation	Measured Results
Isolation		10dBm 16 dBm goal	13dBm	14dBm	TBD
Conversion gain		-2dBm	3.99 dBm	3.55 dBm	TBD
VSWR	RF, LO, IF,	2.5 ;1.5 goal	1.3, 2.0, 300+	1.3, 2, 10	TBD
DC Icc		NA	50mA	50.9mA	TBD
Frequency range		RF 5.725-5.875 GHz LO 5.715-5865 GHz IF .5-20 MHz			TBD

\* Assume all measurements made with a -10dBm RF signal and a -2dBm local oscillator 50 ohms on all ports and a 5 volt power supply.

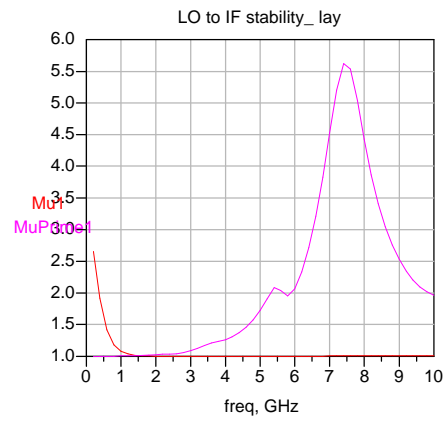
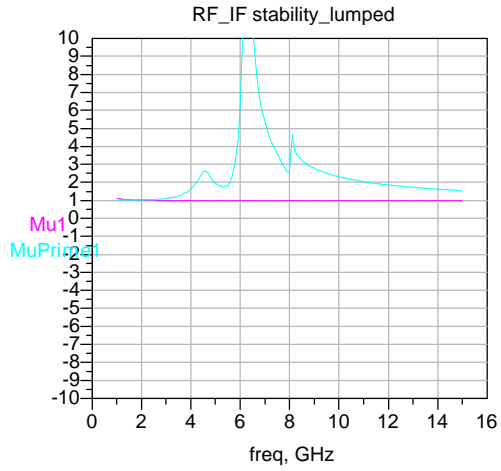
Relevant circuit characteristics.

RF to LO stability Lumped element and Layout figure 11

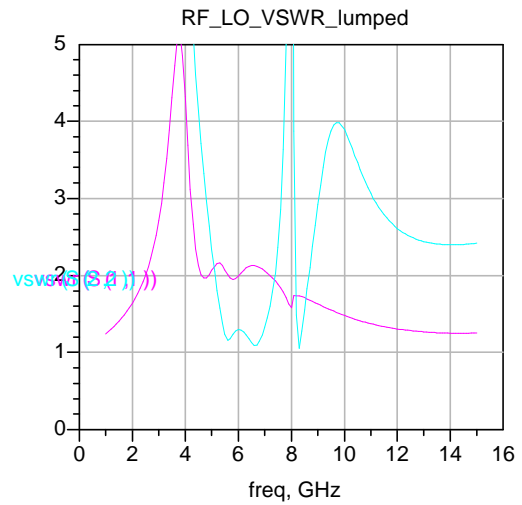
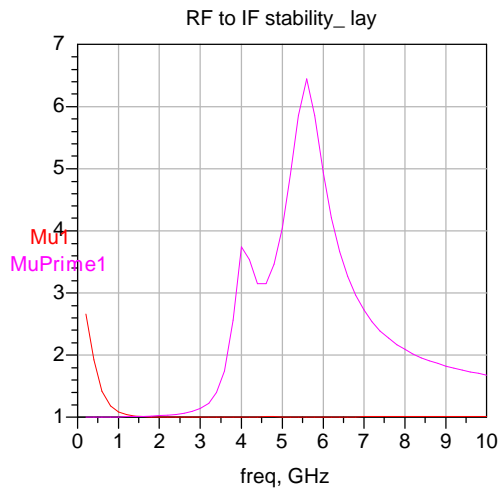
The 3 port S-parameters Lumped element and Layout Figure 13.



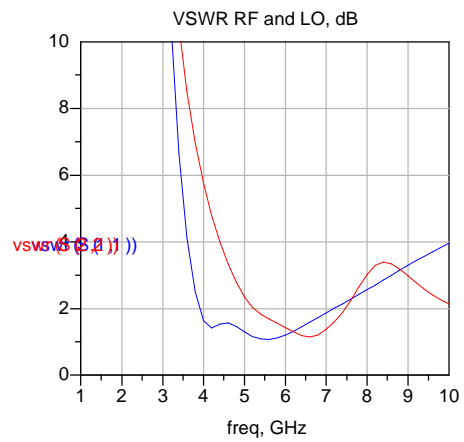
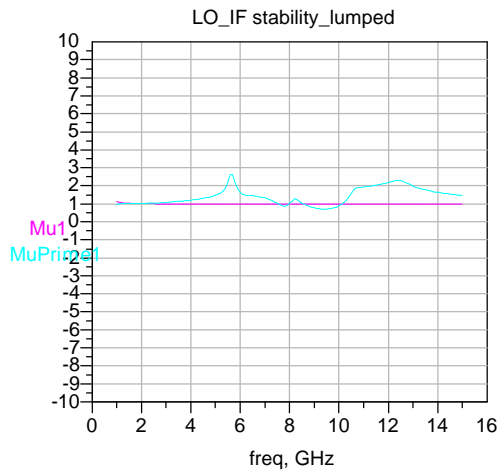
RF to IF stability Lumped element and Layout figure 12



LO IF RF VSWR Lumped element and Layout figure 14.



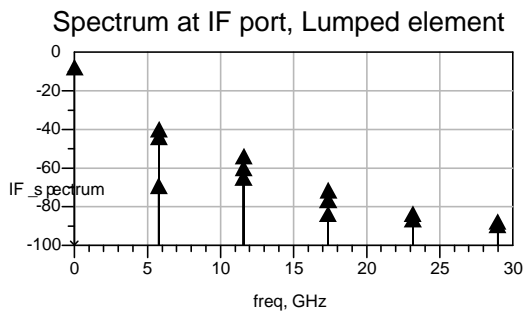
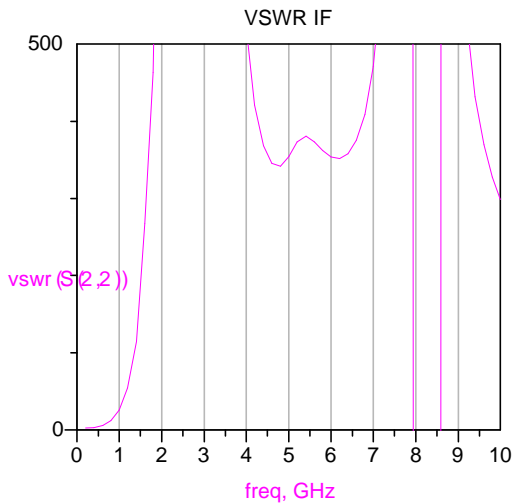
LO to IF stability Lumped element and Layout Figure 13.



## 5. Test Plan

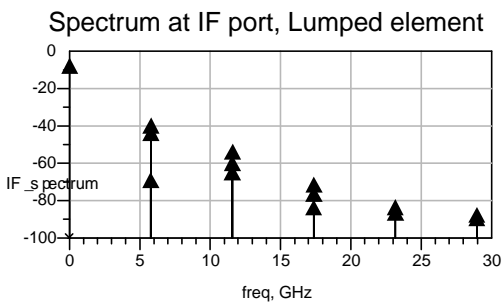
The testing of the mixer will have to be done in three stages; first a power up test, followed by a linear performance test, and concluding with a test of the actual mixing performance. When performing any tests a DC bypass cap or 100nF or more would be recommended near the probe input for additional bypass, and a DC block that will function from 500kHz to 10GHz is necessary on the IF port. The Power up test will require a DC power supply, a spectrum analyzer and two 50 ohm terminations (See figure 16)

IF power spectrum Lumped element and Layout figure 15.



Eqn: IF\_spectrum1=dBm(HB.Vif)

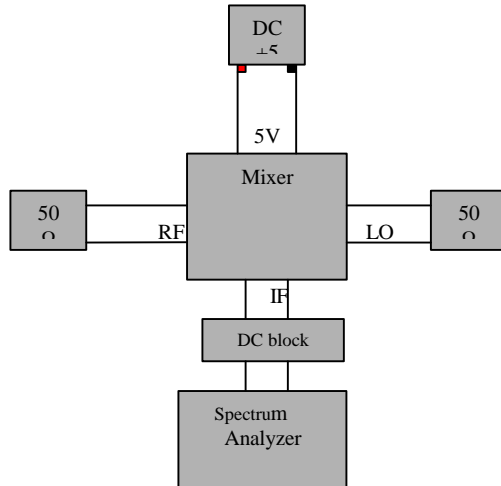
Output Frequency	Conversion Gain, dB
10.00MHz	5.651



Eqn: IF\_spectrum1=dBm(HB.Vif)

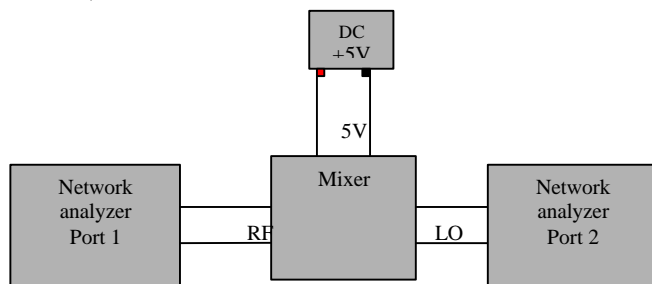
Output Frequency	Conversion Gain, dB
10.00MHz	5.651

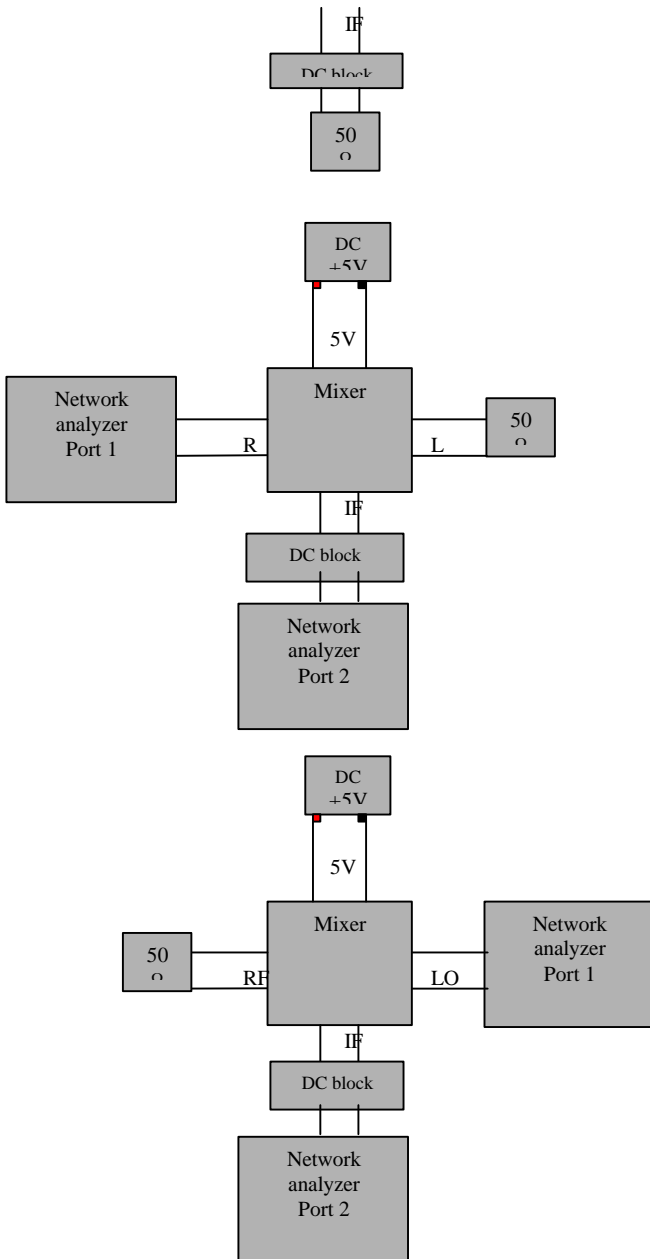
Power on test setup Figure 16.



Upon power up the supply current should be checked to see if the proper current is being drawn (50mA) the spectrum analyzer should be connected to the IF port to check for any oscillations before other tests are performed. After the power up test A liner test should be performed using a network analyzer. A series of the three Two port S-parameter will need to be taken to confirm VSWR and to make sure the frequency performance falls into the expected bands. I would measure between the LO ad RF ports first (See figure 17).

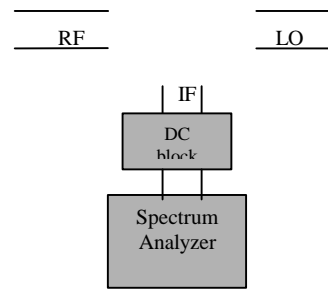
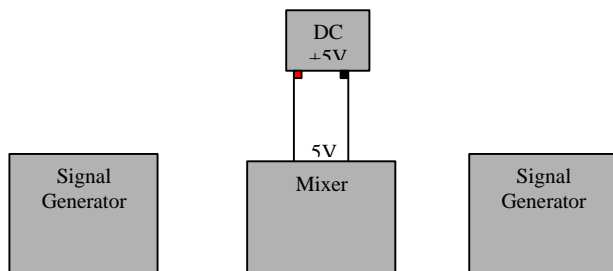
Linear Tests Figure 17.





Look for both the VSWR in the design frequency band and also observe the isolation between the two ports. Next measure the linear parameters between the RF and IF ports noting VSWR and gain/isolation at both the IF and RF frequencies. Perform the same measurements between the LO and IF ports. Finally Using two signal sources and a spectrum analyzer measure the mixing performance (see figure 18).

Mixer test setup Figure 18.



The RF port should be driven at  $-10\text{dBm}$  and  $5.7\text{GHz}$  and the LO port should be driven at  $-2\text{dBm}$  at  $5.790\text{GHz}$ . This will serve to match the measured performance. Measurements at other power levels should be made and variations in the RF and LO frequencies, within the design range should be performed to the degree practical to confirm the performance of the circuit.

## 6. Conclusion and Recommendations

The simulation results seem good considering the design specifications. The VSWR and LO driver requirements and isolation all appear adequate and within spec. The fact that the mixer has significant gain is well beyond what I expected from this circuit. The major concern I am left with is stability. I was unable to design a simulation that guaranteed stability to my satisfaction thus I feel there is a potential for oscillation or some interaction between the stages that was not adequately explored. The measured results will put this issue to rest.

In terms of future work; for this design I think the difference in performance between the Layout simulation and the lumped element simulation shows a great deal of potential for optimization of the layout design. Based on my own experiments I feel there may even be more potential in the lumped element design with proper optimization. These optimizations were neglected at this time due to time constraints and the fact that the current design meets or exceeds the specifications. In addition to optimization and active matching network could be integrated into the follower stage to effect satisfactory VSWR at the IF port.

Improved filtering could be added to the IF output and the matching networks could be redesigned to optimize bandwidth. I believe that all these are possible with out increasing

the size or power requirements of the chip largely through more efficient use of the layout area.

Figure 19 Chip layout

