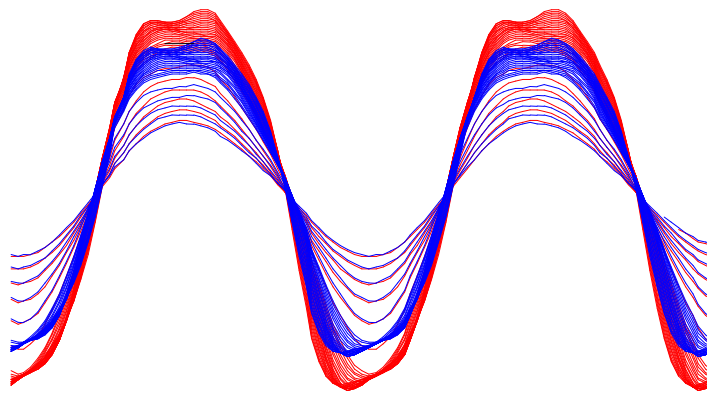


S Band Class F Power Amplifier



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Abstract

A MMIC design for an S-Band Class F Power Amplifier has been realized. This design calls for an efficient amplifier with a bandwidth of greater than 200 MHz with a small signal gain of a minimum of 13 dB and a target of 15dB. The design called for a gain ripple of ± 0.5 dB. The output needed should be greater than 20 dBm @ 1 dB compression point. Additional specifications called for a voltage standing wave ratio 1.5 to 1, an efficiency of greater than 20% at the 1 dB compression point. The design had to be fitted on a 60 x 60 mil chip using TriQuint components.

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Introduction

Circuit Description:

The circuit was realized first with ideal lumped elements and then with TriQuint components and finally with microstrip line connections. The circuit in figure 6 shows the input match, output match, a harmonic trap, bias circuits, DC feeds, and RF short. The input match was realized with C13 and L1. R1 is a stabilizing resistor used for stability. L1 also is used as a RF block for the gate supply. L4 is the drain RF block. C6 and C7 are capacitor used to short any RF signal which reach the supply. C11 and L16 are used to trap the harmonics. C15 is used to match the load and Block any DC voltage from reaching the load.

Design philosophy:

A 600 um TriQuint GFET was chosen with 6 fingers. This is based on which model gives the closest results to actual performance of the transistors. The GFET model was shown in class to give very good result with the gate bias considered. These transistors were also good power handling transistors.

The bias was chosen to about 25 % of I_{dss} . The voltage was chosen based on limitation of the supply. This gave the bias shown in figure 10. The output was matched using the cripps method in order to maximum power across a 50 ohm load. This value was chosen to be ~10 pF. This value later changed due to tuning. The input match was then chosen to give the best match for the transistors and the output power match. This was realized with a ~59 pF cap and a 3.7 nH inductor (L1). L1 was also used as an RF block for the gate supply. Looking at initial results the design was not stable and the R1 resistor needed to be added in order to stabilize the design. This lowered the gain but also stopped to design from oscillating. In order for the design to provide high efficiency, the drain voltage should look like a square wave and the drain current should look like a triangle. The parallel circuit of C11 and L10 were determined in order to trap or block all harmonics except the fundamental. Two additional components were also used in order to short the second harmonic but it was later removed because the values, which were calculated, were unrealizable. He design suffered efficiency loss and let a small portion of the 2nd harmonic to reach the load. The drain voltage waveforms are shown in figure 12. While the current looks similar to a triangle the voltage looks similar to a square. The waveforms could have been improved but that would require handling higher order harmonics. The design was started from the beginning using TriQuint capacitors and resistors. This was done because the TriQuint resistors and mim capacitor give very good performance agreement with ideal elements except for added

resistance. It was determined that using TriQuint components would help stabilize the design with the added resistance associated with each component as well as give good results. The inductors were chosen after the design was completed. The inductors had to be model in order to give the same performance as the ideal results. This is shown in figure 11. The tuning of the harmonic circuits was done in a similar manor. By tuning the harmonic circuits for VSWR and small signal gain the output waveforms were slightly distorted. This is probably due to the inductances changing from ideal to real and being slightly out of tune with each other. The distortions are shown in figure 12. But upon further examination at marker 22, it is showing that the distortion starts at an RF input power of 11 dBm's which is around the same point the design reaches the 1 dB compression point.

Trade-offs:

The trade-off for this design was directly associated with which design specifications were the most important. Initially, meeting the 25% was a goal, which could be reached. Efficiencies as high as ~70% were traded off in order to meet small signal gain. Also in order to stable the design the gain suffered. The VSWR was not met and could not be met and meet the other specifications. Also the efficiency suffered because the higher order harmonics were not addressed. This is because additional components would have made the design too large to fit on the 60 x 60 chip requirement. Also additional components would have brought the small signal gain down further. Another keynote is shown in figure 13 that shows that the 2nd harmonic is actually coming through. This is due to the elimination of the last harmonic circuit.

Modeled Performance

The following compliance matrix shows the specifications given and our results before and after layout.

	Specification	Pre – Layout	Post - Layout
Transistor class	Class F	Yes	Yes
Frequency	2300 to 2500 MHz	Yes	Yes
Gain	13 dB	12.205 dB	12.297 dB
Gain Ripple	+/- 0.5 dB	0.052 dB	0.031 dB
Power out, @ 1dB	20 dBm	23.78 dBm	23.82 dBm
Efficiency	20%, 25% goal	37.175%	37.551%
VSWR	<1.5:1	>1.5:1	>1.5:1
Supply Voltage	+7, -5 Volta	Yes	Yes
Size	ANACHIP	Yes	Yes

From the previous matrix you can see that we are meeting the specification for everything except VSWR and Small signal gain. Our VSWR did not meet the spec however the amplifier is not oscillating. We needed to sacrifice VSWR in order to maintain the more important efficiency and power (figure 1, 3). We just missed the gain spec of 13 dB at 12.2 pre - layout and 12.3 post - layout. We were able to maintain an extremely small gain ripple (figure 1, 3). Our efficiency and power level exceeded our goal by over 10% (figure 2,4).

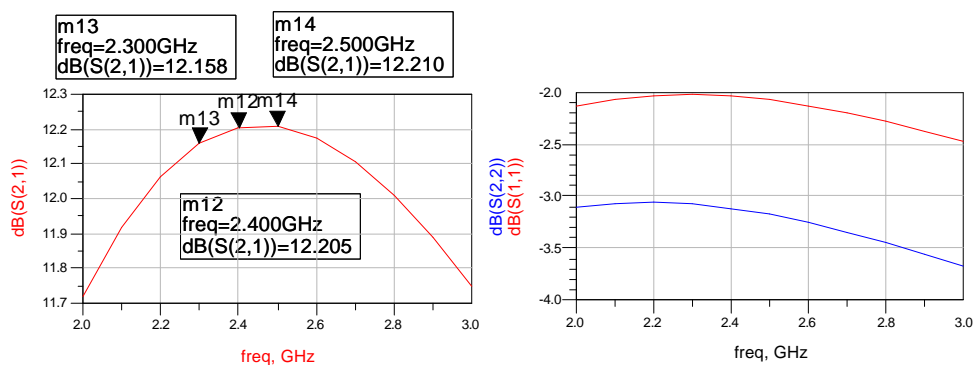


Figure 1

Pre - layout, small-signal responses. Gain, VSWR.

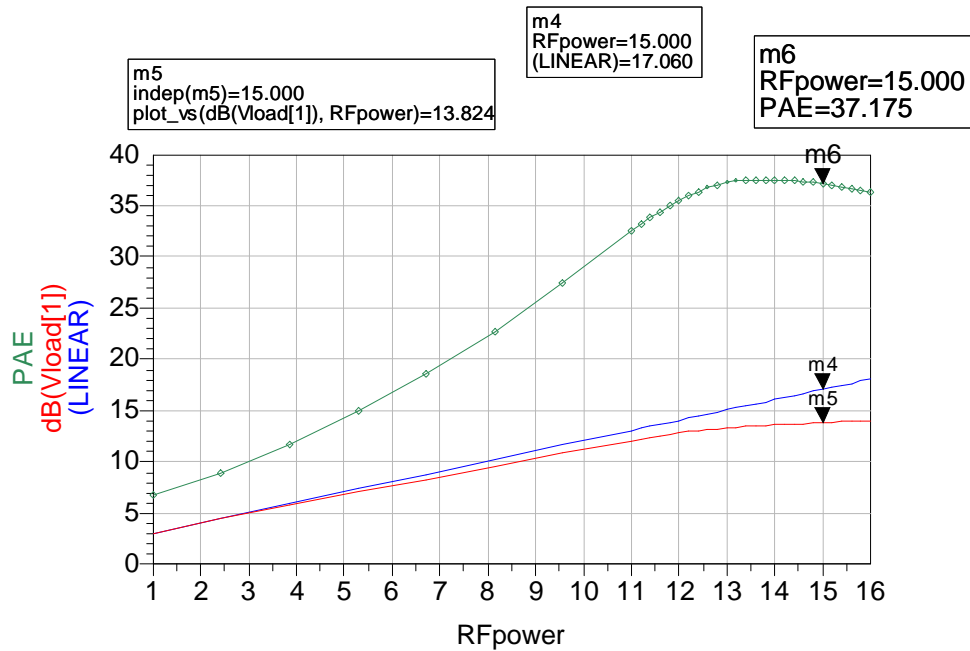
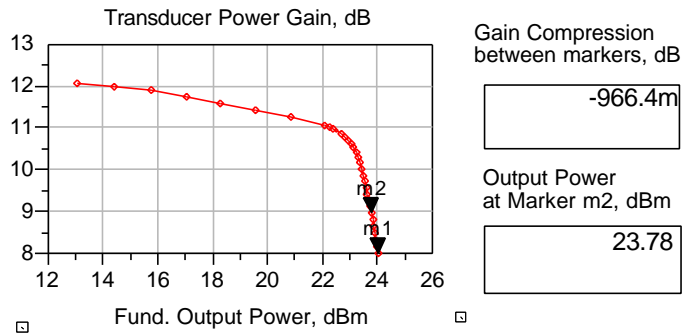


Figure 2

Pre – Layout large – signal responses. Power Added Efficiency, Output power at 1 dB compression point.

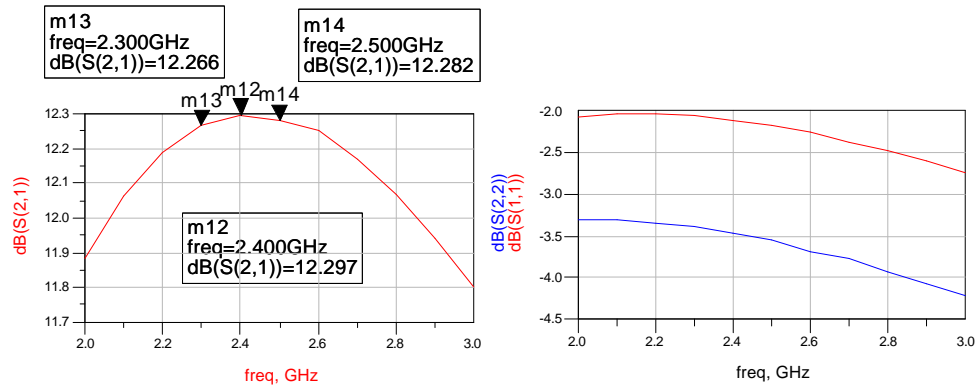


Figure 3
Post – Layout Small signal responses

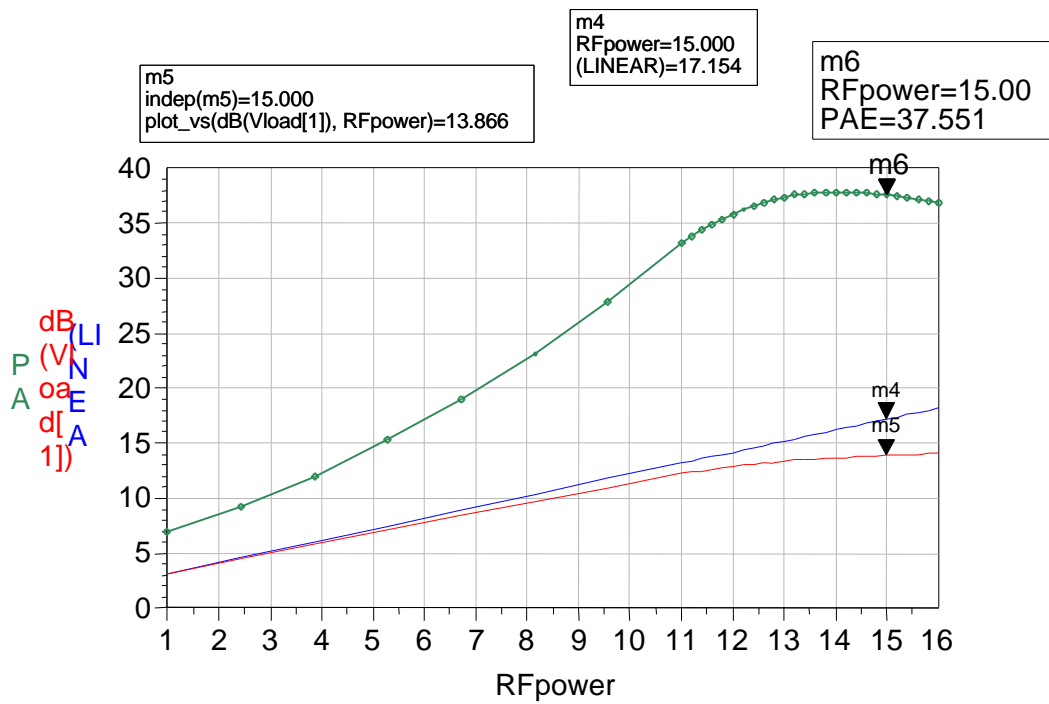
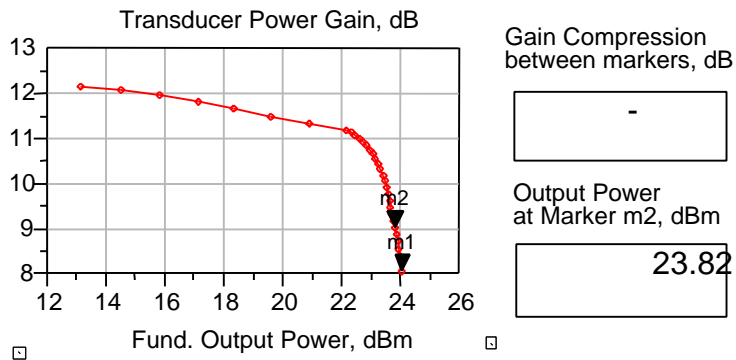


Figure 4
Post – Layout large Signal Responses

Schematic Diagrams and Layout

Simplified Schematic (pre-layout)

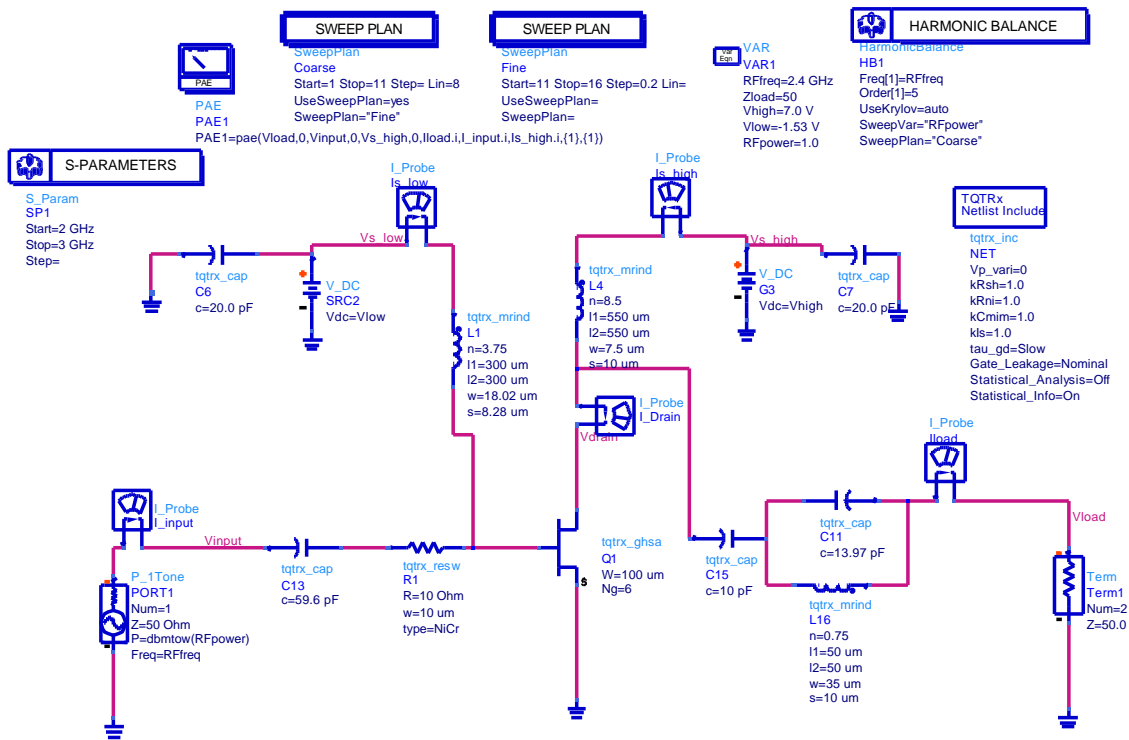


Figure 6
 Schematic (post-layout)

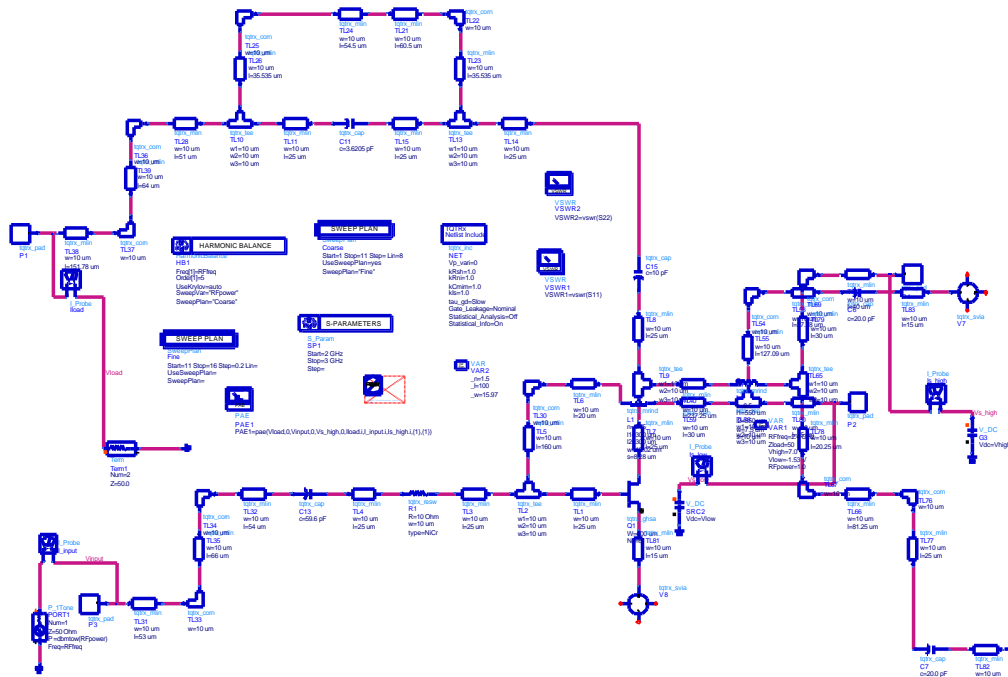


Figure 7

Final Layout

For this layout we tried to keep things simple and use as little space as possible.

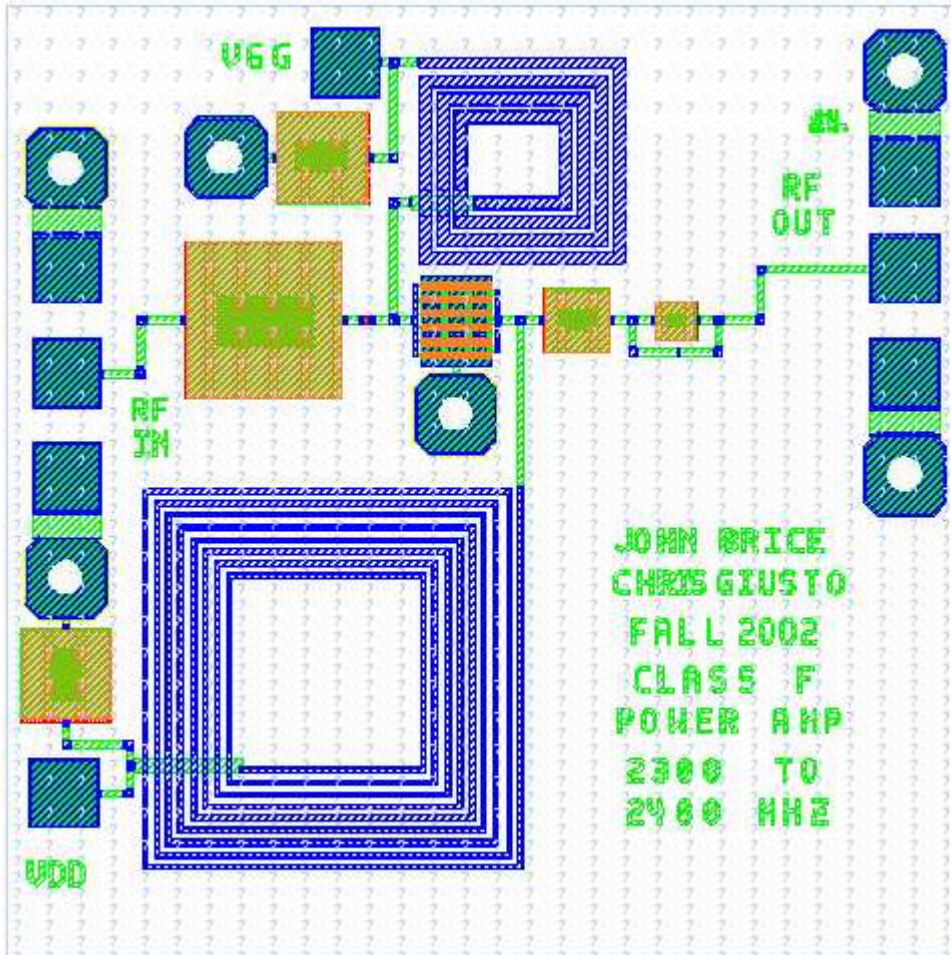


Figure 8

DC Analysis

The following shows DC schematic (simplified) with bias check.

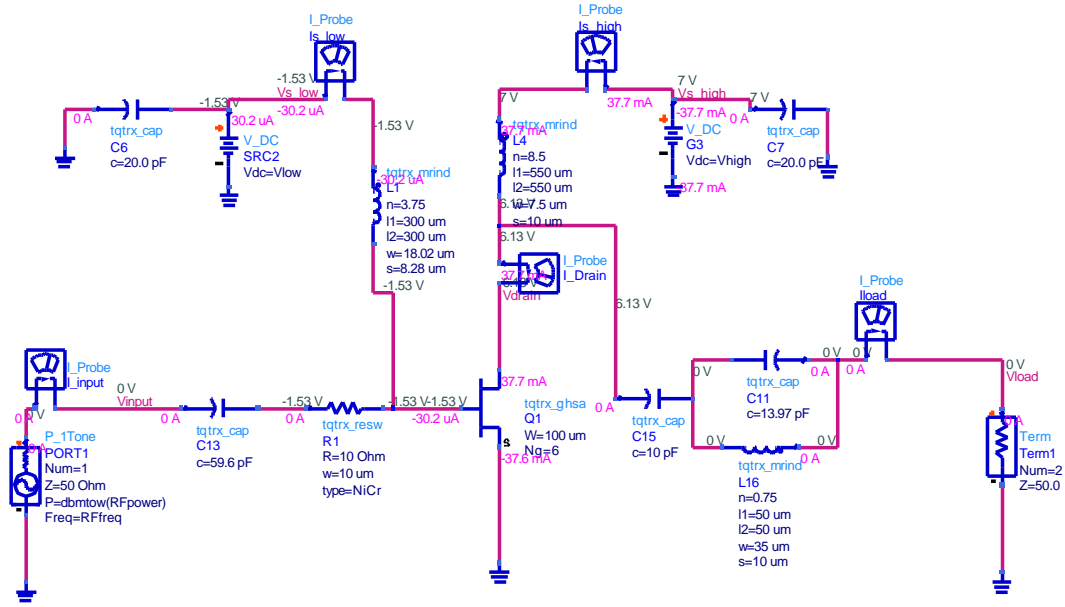


Figure 9

Use with FET_curve_tracer Schematic Template

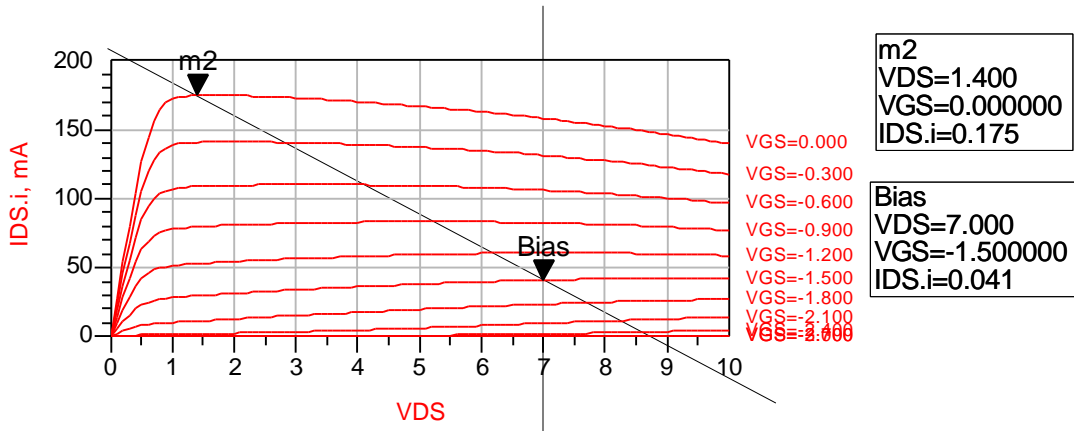


Figure 10

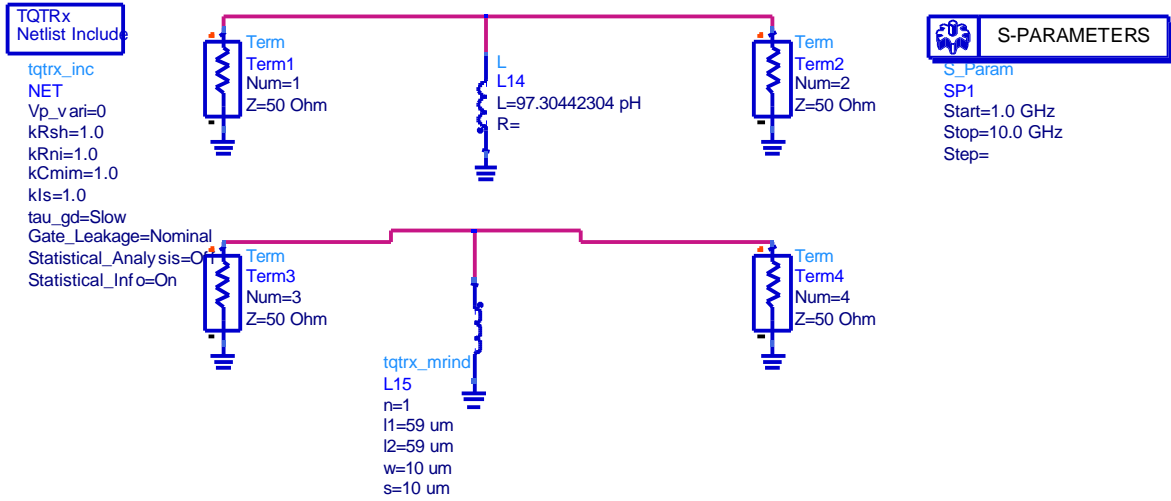


Figure 11

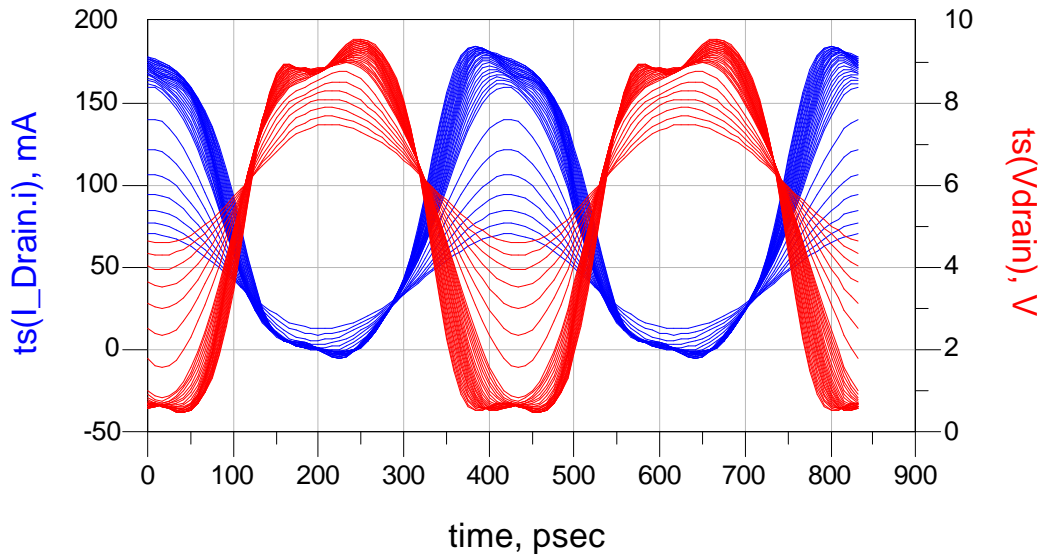
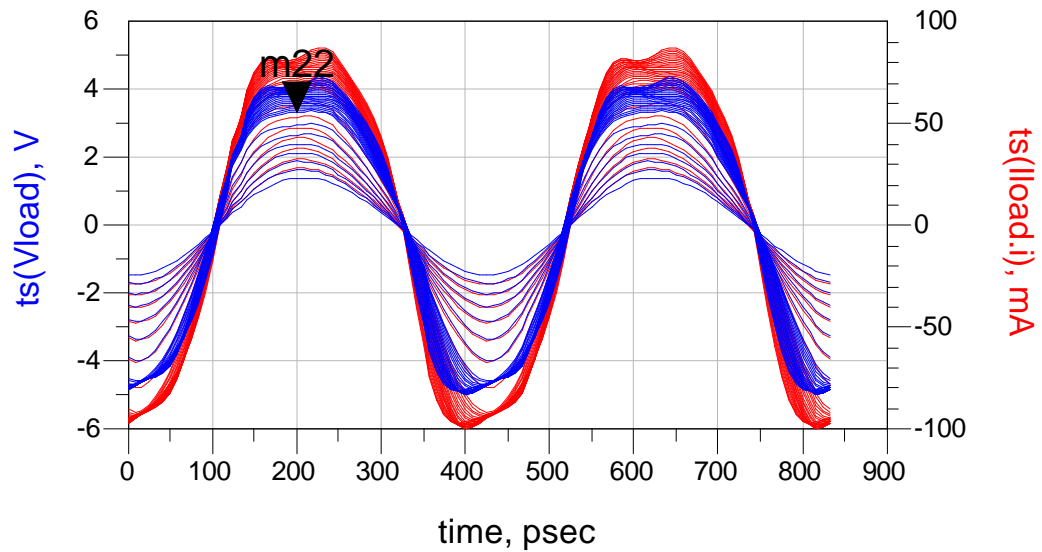


Figure 12



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m22
time=200.0psec
RFpower=11.000000
ts(Vload)=3.324

```

Figure 12 Output Waveforms

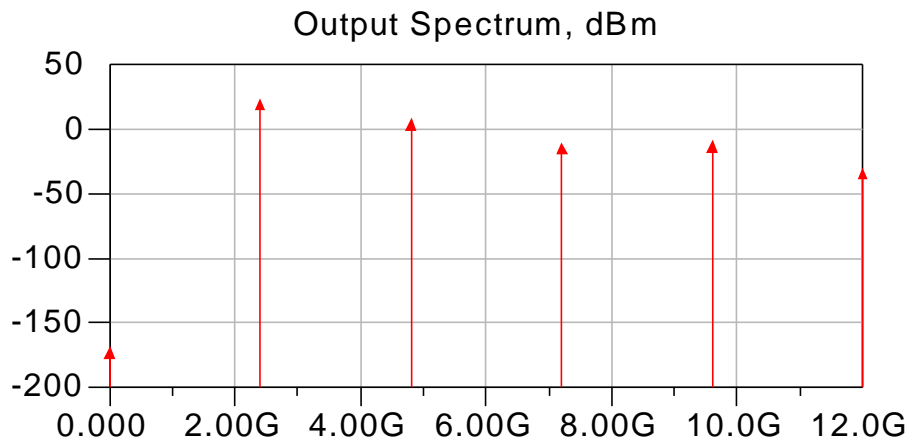


Figure 13 Output Spectrum

Test Plan

Use Cascade probe station to connect the probes to the RF in and RF out ground signal ground pads. Connect the 7 and -5 volt supplies to the VGG and VDD pads respectfully.

Use the VNA 8510 to measure all small signal data. Use a spectrum analyzer along with any needed power meters to measure the large signal aspects.

Conclusion

A class f power amplifier has been realized. Due to the chip size and trade offs all of the required specifications were not met. All of the specifications were met but those, which were not met, came reasonable close. The design was simulated, laid out and analyzed. The design does demonstrate classical class F characteristics and exceed our expectation for this project. This project allowed us to grow as RF MMIC designers.

References

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