

## **1.0 ABSTRACT**

Frequency doublers are the most common application of frequency multipliers due to their high efficiency, circuit simplicity, and minimum generation of unwanted harmonics. The MMIC circuit presented in this paper was designed to double the input frequency band tuned at 2.4GHz – 2.5GHz to 4.8GHz-5.0GHz with isolation for the fundamental and third harmonic  $> 16\text{dB}$ . This frequency doubler will be included in the LO chain of a simplex transceiver for the C-Band Hyperlan wireless local area network (WLAN) system.

## **2.0 INTRODUCTION**

### 2.1 Circuit Description:

This MMIC circuit consists of a frequency generator (X2), band reject filters at the fundamental and the third harmonic frequency and a bandpass filter. The nonlinear component used to generate an output signal rich in harmonics is the Triquint 300um GFET device. There is a stabilizing resistor at the input. A double supply scheme was employed to provide the proper bias to the device.

### 2.2 Design Philosophy:

The initial phase in the multiplier design is determining the feasibility of the desired performance from the specifications given. In order to do this, it was necessary to check the characteristics required from the active and passive elements that would be used to achieve the specified performance. Knowing that the multiplier design is a function of the active device's nonlinear characteristics, it is important to choose the right device based on the frequency of operation, level of input drive, bias conditions and terminations at the fundamental frequency, and its ability to generate harmonics. For this design, the 300um

GFET device was chosen and biased to operate close to pinchoff where  $V_{DS} = 5V$  and  $V_{GS} = -1.85V$ . The bias was chosen in pinchoff because in the vicinity of pinchoff a half-wave rectified sinusoidal current is generated that is rich in even harmonics. Next, it was important to design optimum input and output matching networks such that the input network is matched to the fundamental and the output network is matched to the second harmonic. The input matching network employ simple series L and shunt C topology and the output matching networks employ a simple series L topology. However, since microwave transistors are active devices with intrinsic feedback, it was necessary to check the stability of the device over a wide frequency range (.5GHz – 8GHz). After checking the stability of the device, there was noticed that within the low frequency range the device was unstable. A shunt-stabilizing resistor was incorporated at the input to increase the device's stability performance over a wide range of frequencies. The gate bias was applied to the stabilizing resistor with another simple LC network that contained a 10pF capacitor and 6pH inductor. An output filter section was needed to reject the fundamental and third harmonics. Two bandreject resonator sections were designed on the output to prevent low frequencies and frequencies higher than  $2f_0$  from being amplified by the device. The band reject resonator for  $f_0$  along with a resistor divider was used to supply the appropriate bias to the drain. Finally, a bandpass filter incorporating one resonator was added in cascade with the bandstop filter in order to achieve the desired output response.

### 2.3 Tradeoffs:

There are several tradeoffs to the particular design chosen. By fine tuning the input and output circuits to achieve maximum input VSWR at the fundamental and maximum output VSWR at the second harmonic frequency, this approach results in a narrow-band multiplier, exhibiting less than 10% fractional bandwidth. Due to the size constraints, no output amplifier design was employed to boost the output power at the second harmonic. This in turn resulted in low conversion gain of

-6dB. The biasing conditions were not optimum for this type of design. Operating closer to pinchoff would introduce stronger effects of the harmonics at the output. Due to the limitations of the nonlinear model, the operating point had to be slightly above pinchoff in order to achieve consistent results.

The bandpass resonator at the output increased the bandwidth of the design, however, it wasn't symmetric about the operating frequency band. Employing an output amplifier would cause the design to be more centered about the operating frequency and possibly eliminating the need for a bandpass filter. Utilizing a single supply topology would allow for an output amplifier, however, due to conversion problems with the simulator, a double supply topology was utilized instead.

### 3.0 MODELED PERFORMANCE

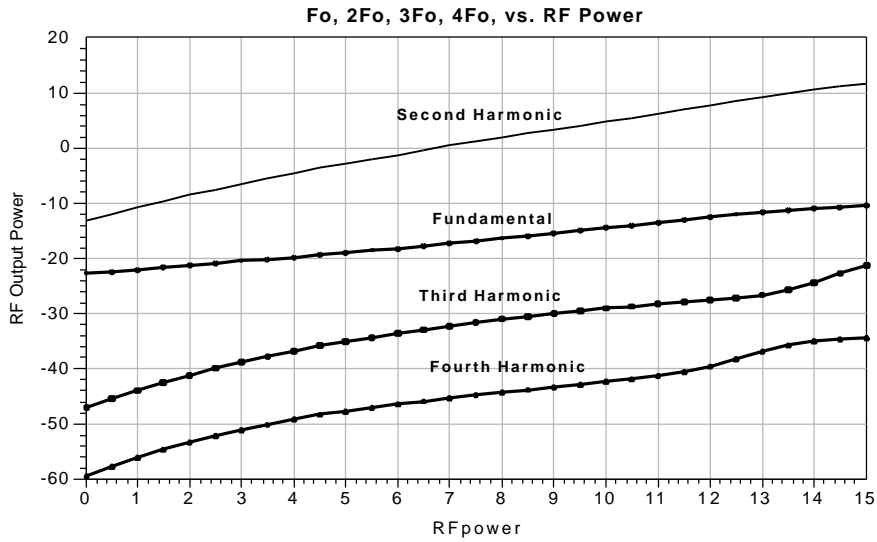
The following table gives information concerning the original specifications and the modeled results.

	Original Spec	Result Before Layout	Result After Layout
<b>Frequency</b>	Output= 4.8GHz-5.0GHz Input = 2.4GHz-2.5GHz	input= 2.4GHz-2.8GHz output= 3.5GHz-5GHz	input= 2.4GHz-2.8GHz output= 3.5GHz-5GHz
<b>Conversion Loss</b>	3dB,max; 0dBgoal	-6dB	-6dB
<b>Input Power</b>	+ 10dBm	+ 10dBm	+ 10dBm
<b>Isolation</b>	fo= 16dB,min: 25dB, goal 3fo= 20dB,min: 30dB, goal	fo= -19dB, 3fo= -33dB	fo= -19dB, 3fo= -33dB
<b>VSWR, 50</b>	2.5:1,max.; 1.5:1, goal	1.3:1,out.; 1.0:1, in	1.1:1,out.; 1.1:1, in
<b>Supply Voltage</b>	+ 5V, -5V; + 5, only	+ 6.5V, -1.85V	+ 6.5V, -1.85V
<b>Size</b>	60 X 60 mil	60 X 60 mil	60 X 60 mil

Table 3.1 Original Specifications vs. Modeled Performance

Conversion loss could have been attainable with an additional output amplifier, however, due to size limitations, this was not a viable option. The operating frequency band is sensitive to the output filter with a maximum input

match at 2.5GHz and maximum output match at 4.9GHz. The output filter added 2dB of loss to performance.



The following plots illustrate the simulated performance after layout.

Figure3.1 Output power of first 4 harmonics.

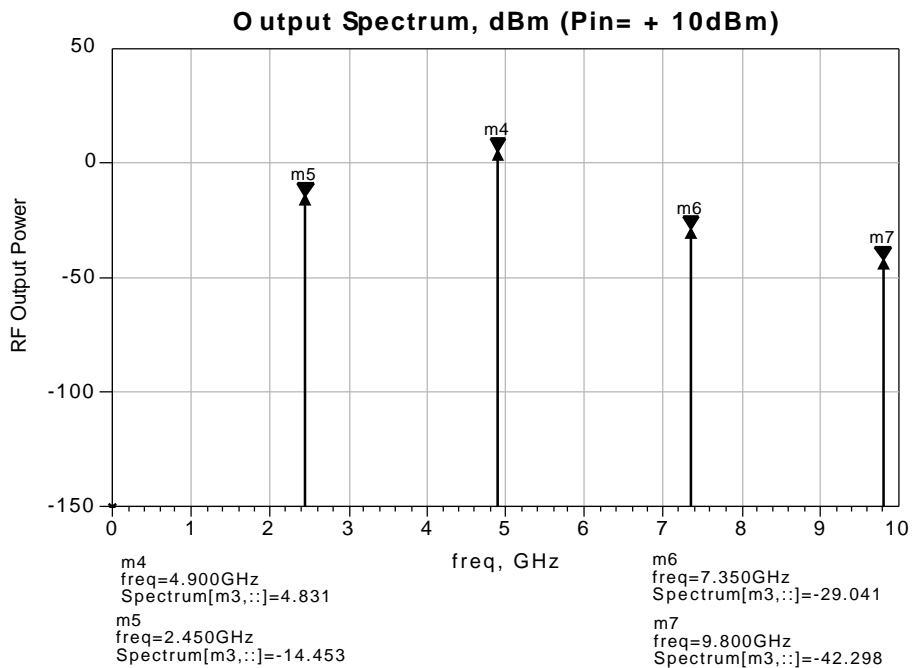
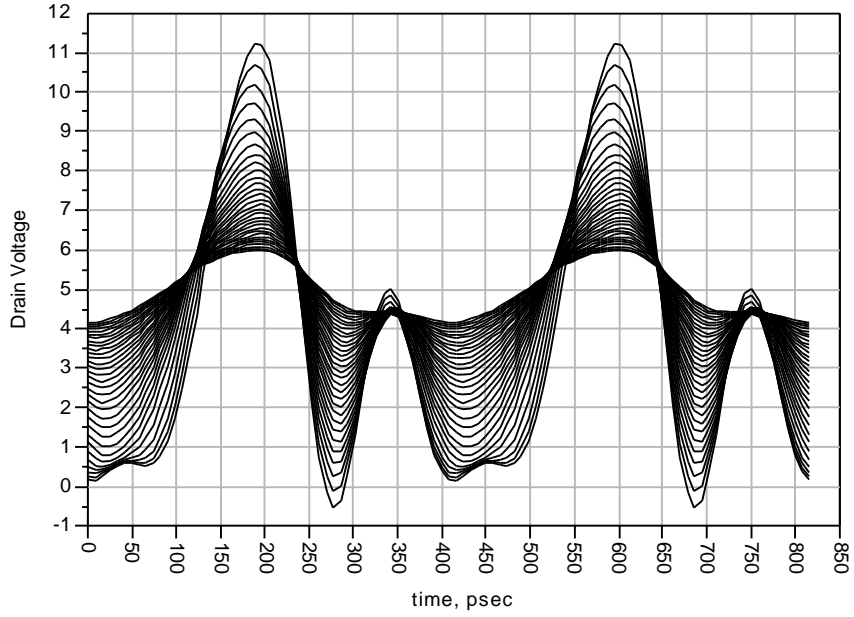


Figure3.2 Output power spectrum of first 4 harmonics

Figure3.3 Output Voltage Waveform (for  $0\text{dBm} > P_{in} > +15\text{dBm}$ )  
**O**utput Voltage **W**aveform



**O**utput **C**urrent **W**aveform

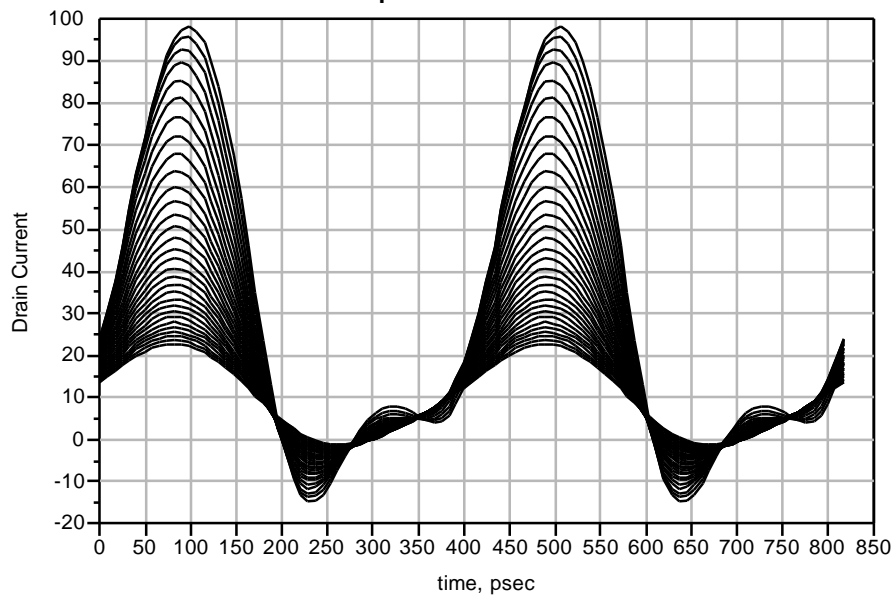


Figure3.4 Output Current Waveform (for 0dBm>Pin> +15dBm)

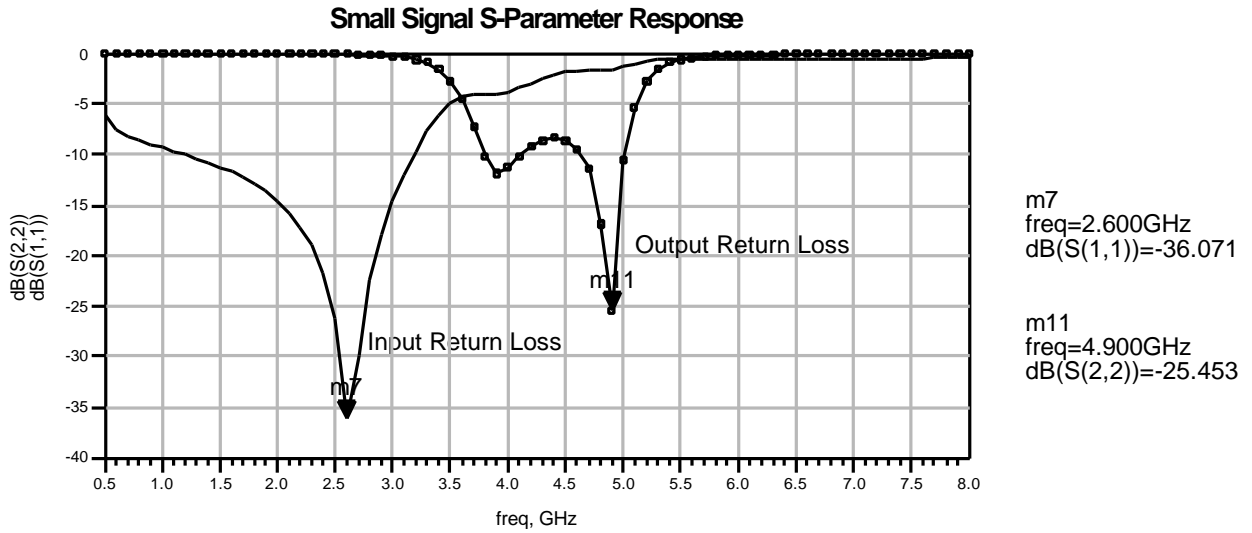
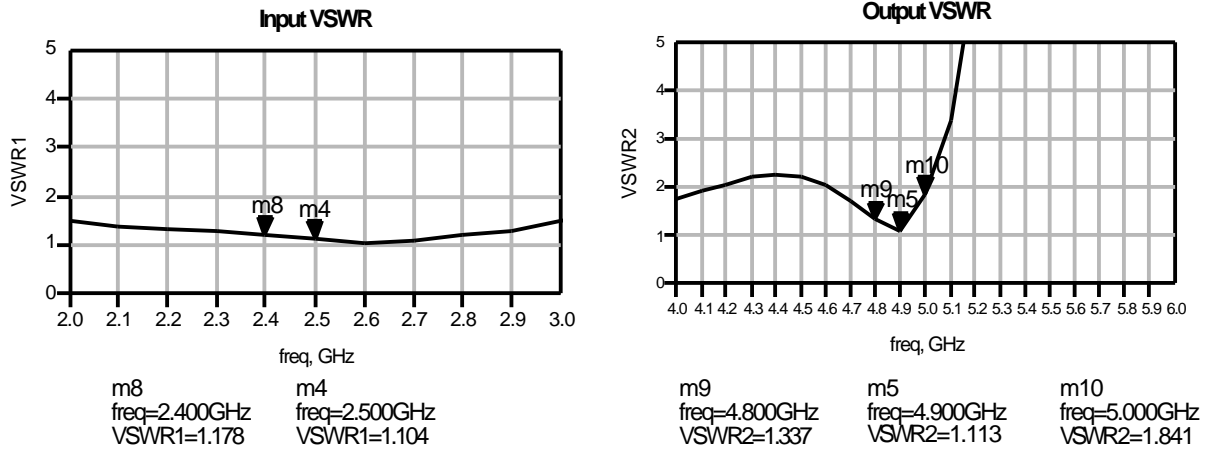


Figure3.5 Input and Output Match Results

Figure3.6 Input and Output VSWR Results



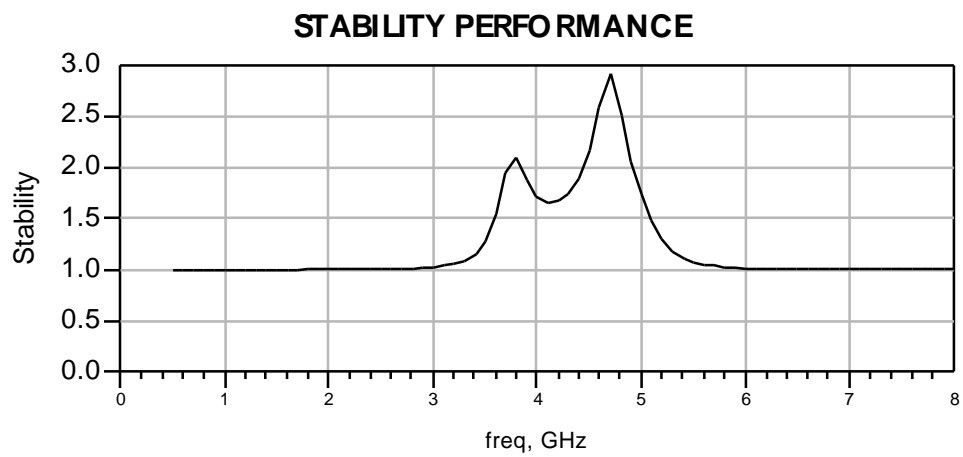


Figure3.7 Stability Performance over extended frequency band.

## 4.0 SCHEMATIC DIAGRAM

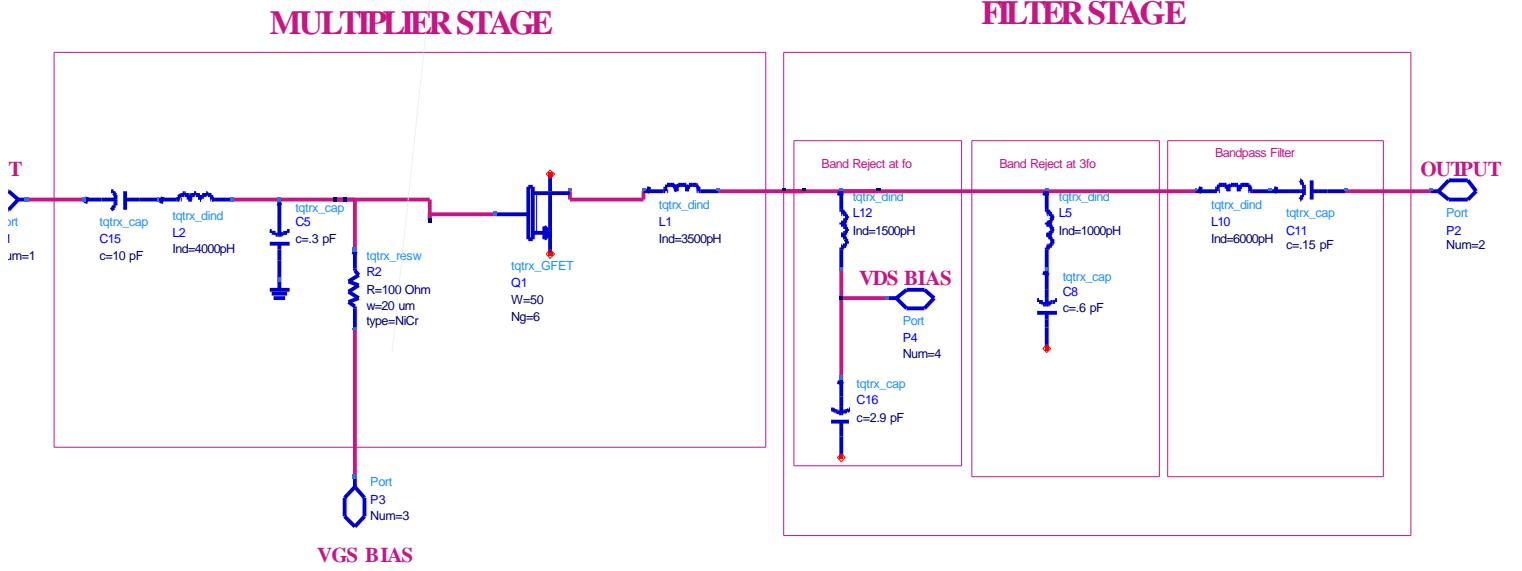


Figure4.1 Simplified Schematic Diagram

## 5.0 DC ANALYSIS

(See Appendix A for simplified DC Schematic)

The +6.5V source applied to the drain measures 22mA of current dc and 8.5mA of ac current and the -1.85V source applied to the gate measures 10uA of current. There is an expected current swing of up to approximately 65mA and a voltage swing of up to 8V with supplied input power of +10dBm. The MIM capacitor breakdown voltage is around 10V and the maximum current carrying capacity for the spiral inductors is 180mA. In addition the NiCr resistors utilized in the resistor divider are 105um in width and are more than capable of handling the current capacity specified at 1mA/um. The interconnections between Metal1 and Metal 2 combined are able to handle 27mA/um of current. The DC lines are 10um.

## 6.0 TEST PLAN

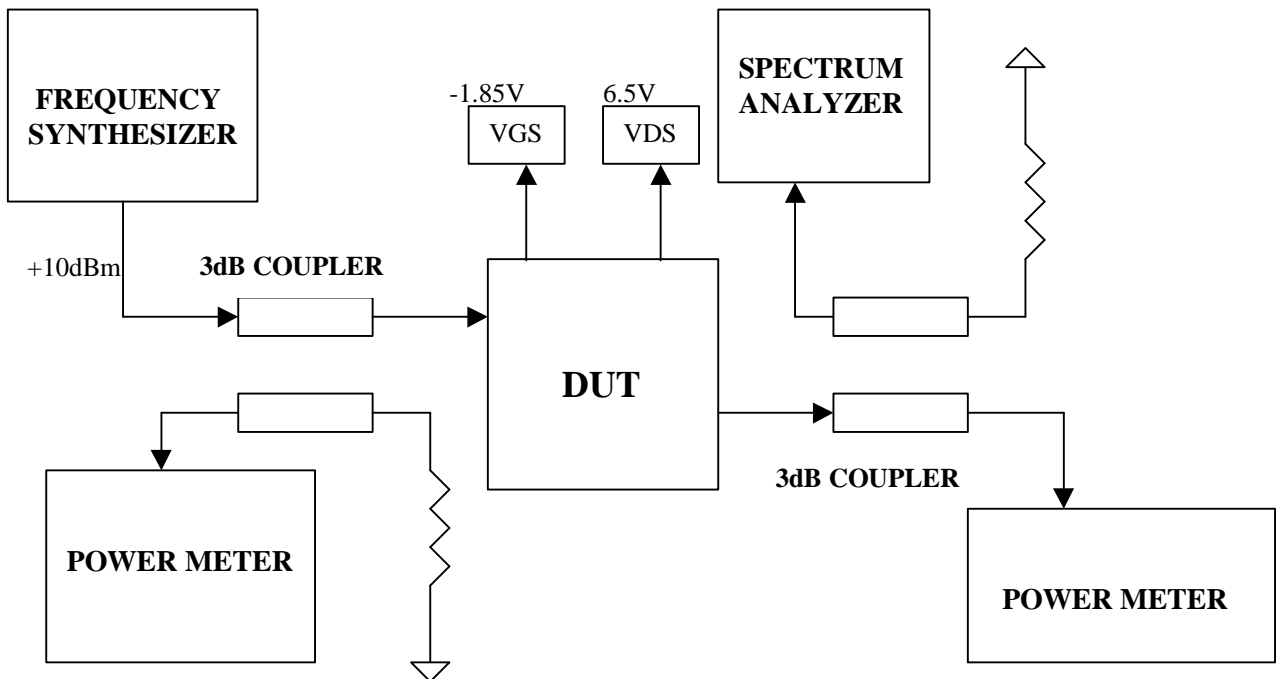


Figure6.1 Abbreviated harmonic test plan.

The above figure illustrates an abbreviated test plan that can measure the harmonic performance of the multiplier circuit. To test the small signal performance of the circuit design a network analyzer can be replaced at the input and output ports of the multiplier.

## **7.0 CONCLUSIONS AND RECOMMENDATIONS**

In conclusion, this multiplier design is very sensitive to the output filter section. Any slight variance in the capacitance within  $\pm 0.01\text{pF}$  the response of the filter is greatly affected. In a second pass design, a better filter section would need to be implemented to decrease sensitivities and losses added to the circuit. In addition, a self-bias scheme could be employed in order to increase available space on chip. In turn, the available space would allow for an output amplifier that would boost the conversion gain at the second harmonic at the required RF input drive.

## APPENDIX A

## APPENDIX B

Multiplier X2 Layout

## REFERENCES

Camargo, E., *Design of FET Frequency Multipliers and Harmonic Oscillators*, Boston, MA: Artech House, 1998.

Maas, S., *Nonlinear Microwave Circuits*, Norwood, MA: Artech House, 1988.