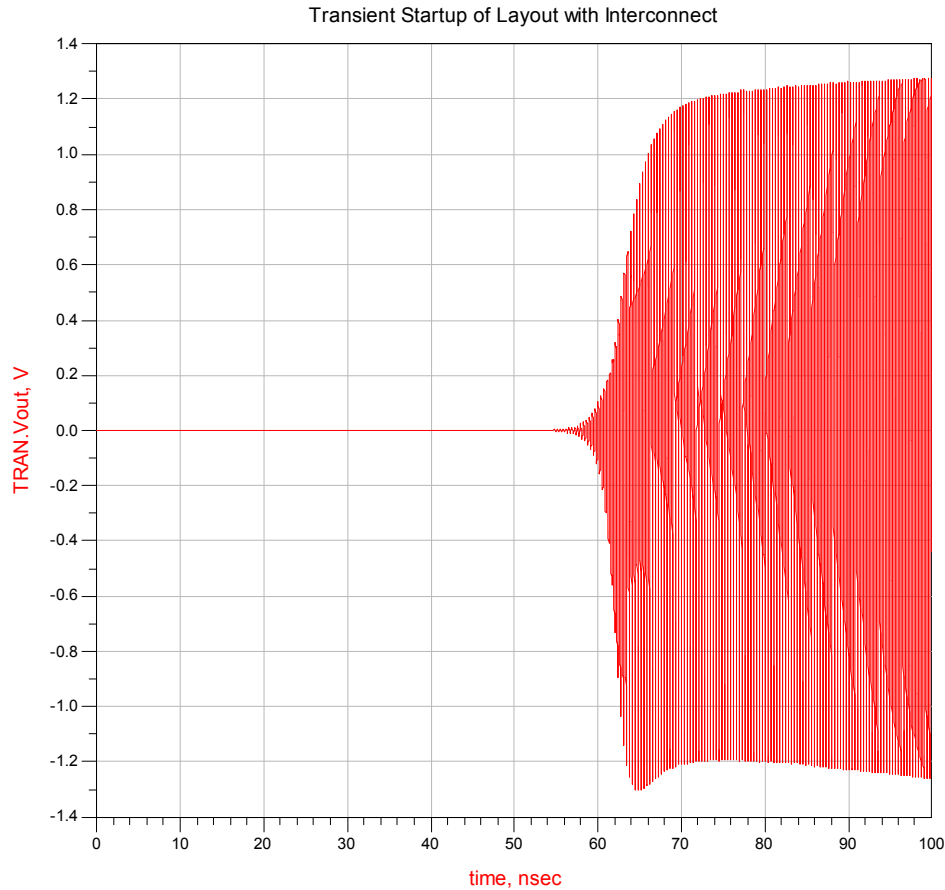


An S – Band, 0.6- μm GaAs, Voltage Controlled Oscillator



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I. Summary

An approach for the design of an S-Band Voltage Controlled Oscillator (VCO) for application in HyperLAN and ISM systems implemented in Triquint TQTRx 0.6- μm GaAs technology is presented. The VCO operates from 2596 MHz to 2893 MHz with output power ranging from 14.287 dBm to 12.259 dBm respectively. The VCO powered by a 5 Volt supply, features an on chip high Q resonator and tuning varactor controlled with a 0 to 5 Volt variable supply. The VCO has been used in the design of a frequency converter for a C-band HyperLAN simplex transceiver.

II. Introduction

A. Circuit Description

A simplex MMIC transceiver implemented in the Triquint TQTRx process (4 mil thick GaAs) with simulation and layout in Agilent ADS (ADS version 150) has been designed for C-Band HyperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequency applications.

The system utilizes a C-Band Up-Down Converter with a 275MHz intermediate frequency (IF) that can be down-converted to baseband with a second 275MHz local oscillator (LO). The second LO is upconverted to the C-Band in TX mode and modulation can be introduced onto the second LO or through direct frequency modulation of the VCO in the transceiver. The dual band usage VCO with high side or low side (HSLO/LSLO) injection to the mixer is specified for operation from 2712 MHz to 2813 MHz, which when doubled is between the WLAN and ISM frequencies.

Receive and transmit signals are routed by C-Band single-pole-double-throw (SPDT) switches. The receive chain consists of a cascaded low noise amplifier (LNA) and post amplifier. The transmit path employs a variable gain amplifier for level control and a driver amplifier preceding a 0.25 Watt power amplifier.

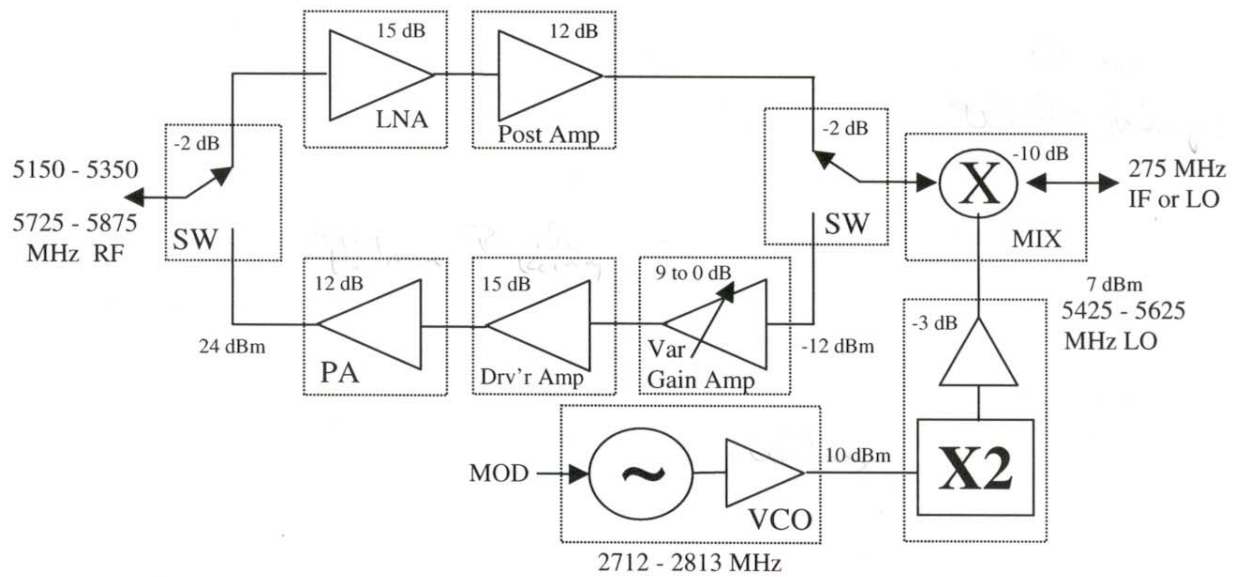


Figure 1. Chip-Set for the 5150 – 5350 MHz WLAN and 5725 – 5875 MHz ISM Bands.

The 5 Volt powered, 0 to 5 Volt voltage controlled oscillator, as shown in Fig. 2, operates from 2596 MHz to 2893 MHz with output power ranging from 14.287 dBm to 12.259 dBm respectively, while occupying only a 60 x 60 mil Anachip area. The VCO features a self-biased, $W=50\mu\text{m}$, $N=6$, TQTRx_DFET with an active current source utilizing a gate to source tied inductor for frequency dependent gain control which minimizes higher order harmonic components at the output. Common-source capacitive feedback is employed in the design to satisfy the required oscillation criteria with a series resonance applied at the gate of the VCO FET. The required output power is achieved by a $W=70\mu\text{m}$, $N=8$ source follower output stage.

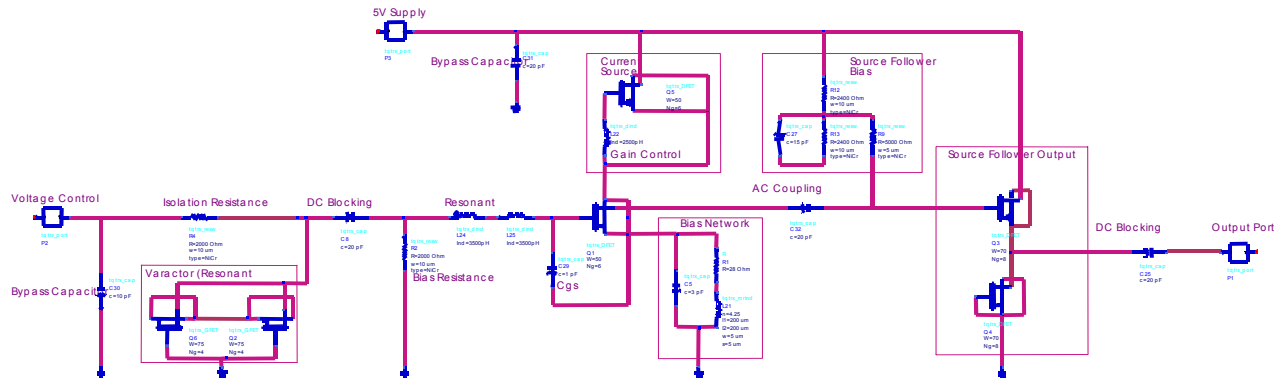


Figure 2. VCO Block Diagram.

B. Design Philosophy

The VCO architecture is based upon small signal negative impedance theory where the active circuit is represented by the impedance,

$$Z_a = R_a + jX_a$$

and the load circuit as

$$Z_1 = R_1 + jX_1$$

as shown in Fig. 3. Assuming that a steady state oscillation is occurring between the two networks then there must exist a loop current, I , that is non-zero. Using Kirchoff's law, the total loop voltage then must be zero which yields

$$Z_a + Z_1 = 0.$$

It can therefore be observed that

$$Z_a = -Z_1 \text{ (negative impedance)}$$

to ensure oscillation and hence the nomenclature of the theory and design technique. Furthermore, in small signal design, the imaginary portion of this relation is of particular interest and thus

$$X_a + X_1 = 0.$$

The large signal operation of a FET oscillator can then be predicted from its small signal characteristics since as the signal grows to steady state, the actual change of the imaginary portion of the active circuit is small.

The differential change in the active circuit impedance versus the operating point amplitude and frequency delta variations as described by Kurokawa is then,

$$[dR_a/dA][dX_1/d\omega] - [dR_1/d\omega][dX_a/dA] > 0$$

where R_a is the active device's negative resistance, A is the steady state amplitude, and ω is the frequency. As stated earlier, the change in X_a with respect to amplitude is small and considered to be zero. However, for GaAs FET oscillators, R_a increases positively with respect to amplitude since the negative resistance of the circuit decreases in magnitude with increasing amplitude. Therefore applying these conditions, then

$$[dX_1/d\omega]_{\omega_0} > 0$$

which implies that stable oscillations are ensured when the reactive component of the load impedance has a positive slope versus frequency, and the frequency of the oscillation corresponds to the zero crossing of the frequency axis.

Additionally, it has been shown that for a series resonant oscillator that

$$|R_a| \sim \geq 3R_1$$

to approximate a power impedance match between the load circuit and the large signal steady state oscillations. The factor of 3 is itself a compromise based upon the experimental trade-off between start-up conditions and final oscillation frequency.

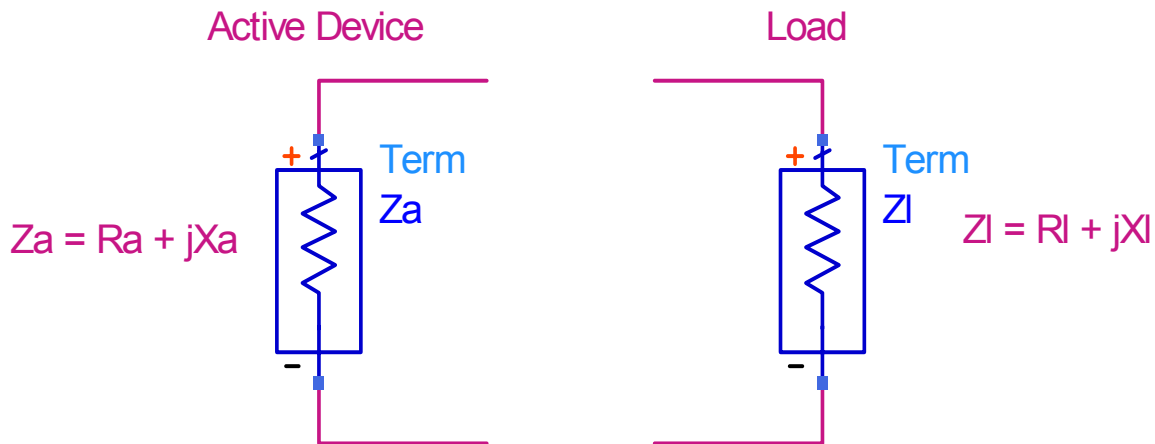


Figure 3. Conditions for oscillator startup.

To provide suitable output power for further amplification in a subsequent stage to achieve the output power specification, a $300\mu\text{m}$ ($W=50\mu\text{m}$, $N=6$) DFET (TQTRx DFET nonlinear model) was used to implement the oscillator and self-biased with a source resistor. The active current source is biased to provide $\sim 12\text{mA}$ to the oscillator FET and has an inductor tied between the gate and source to effect a rudimentary form of frequency dependent gain control. This is because at higher frequencies, the inductor opens up and tends to choke off current from the oscillating FET. This was added to help reduce the higher order harmonic component of the

output since otherwise the oscillations become limited. Additionally, the 5 Volt supply of the current source includes a 20pF bypass capacitor.

Common-source capacitive feedback sets the frequency of oscillation as given by

$$F_{osc} \cong [2\pi * \{L_r * (C_{VAR} || C_i)\}^{0.5}]^{-1}$$

where

$$C_i = (C_{gs} * C_f) / (C_{gs} + C_f)$$

and based upon start-up conditions, C_f was chosen to be 1pF.

The oscillator employs a series resonance at the gate to realize the negative resistance and was implemented as two 3500pH series inductors rather than one for ease of layout and tuning ability.

The Triquint varactor is implemented by two parallel 300 μ m ($W=75\mu$ m, $N=4$) GFET's with drain and source tied together and modeled as a parallel combination of a 0.04pF capacitor and a 5 Ω resistor in series with the tuning capacitor as shown in Fig. 4. (See Tuning Range in Fig. 5.) As a tuning voltage is increased on the tied drains, the depletion regions of the FET's are likewise increased. This causes an increase in the distance between the effective plates of the capacitor like structure and thus the capacitance decreases. A decrease in capacitance causes the oscillator to subsequently oscillate at a higher frequency with the converse true as well.

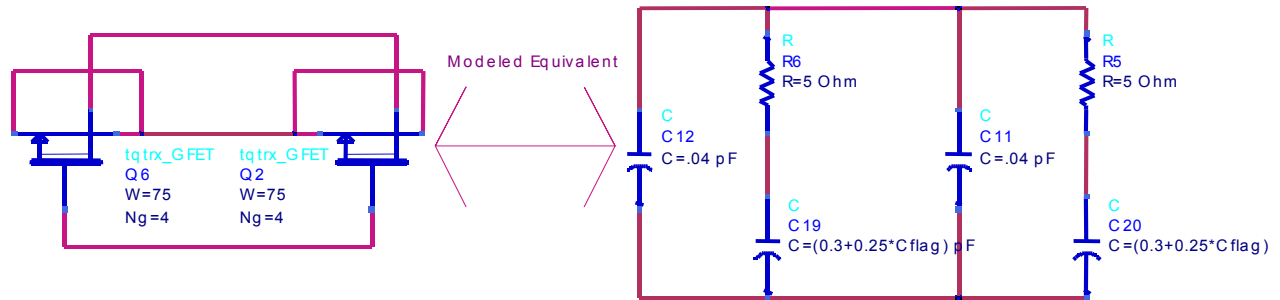


Figure 4. Varactor model.

Bias Voltage (V)	Tuned Capacitance (pF)
0	0.55
1	0.4
2	0.3

Figure 5. Single Varactor tuning range; 300 μ m ($W=75\mu$ m, $N=4$) GFET.

The input network also includes a series 20pF DC blocking capacitor, a 2K Ω resistor for isolation, and a 20pF bypass capacitor to filter power supply noise.

The oscillator FET is then AC coupled with a 20pF capacitor to a 560 μ m source follower output stage which provides the additional gain required for the output power specification. The source follower was implemented with a $W=70\mu$ m and $N=8$ DFET to support the large bias current required to meet and or exceed the greater than 10dBm output power goal. It is biased with a resistor divider network at the gate and a $W=70\mu$ m, $N=8$ DFET with gate tied to source. Additionally, the 5 Volt supply, which is applied to the resistor divider network, includes a 20pF bypass capacitor (same 5 Volt supply for the oscillator FET current source). A series 20pF capacitor was again added as a DC block at the output. The entire VCO architecture is illustrated in Fig. 2.

C. Trade-Offs

There were three major trade-off scenarios in the design of this VCO.

The first trade-off encountered was the inability to use an inductive load in the first stage of the VCO. This resulted from simulator convergence problems and rather than jeopardize the confidence level of the simulation results actually matching the fabricated circuit, the design was adapted to use a current source load so results could be better predicted with the simulator.

Design compromises were also made between the gain of the VCO and the contributions of harmonics at the output. The gain required to satisfy the start-up conditions was contrasted against the signal limiting occurring at the drain of the oscillator FET and at the output of the source follower stage, as signal compression resulted in an increased harmonic component in the output and decreased power efficiency.

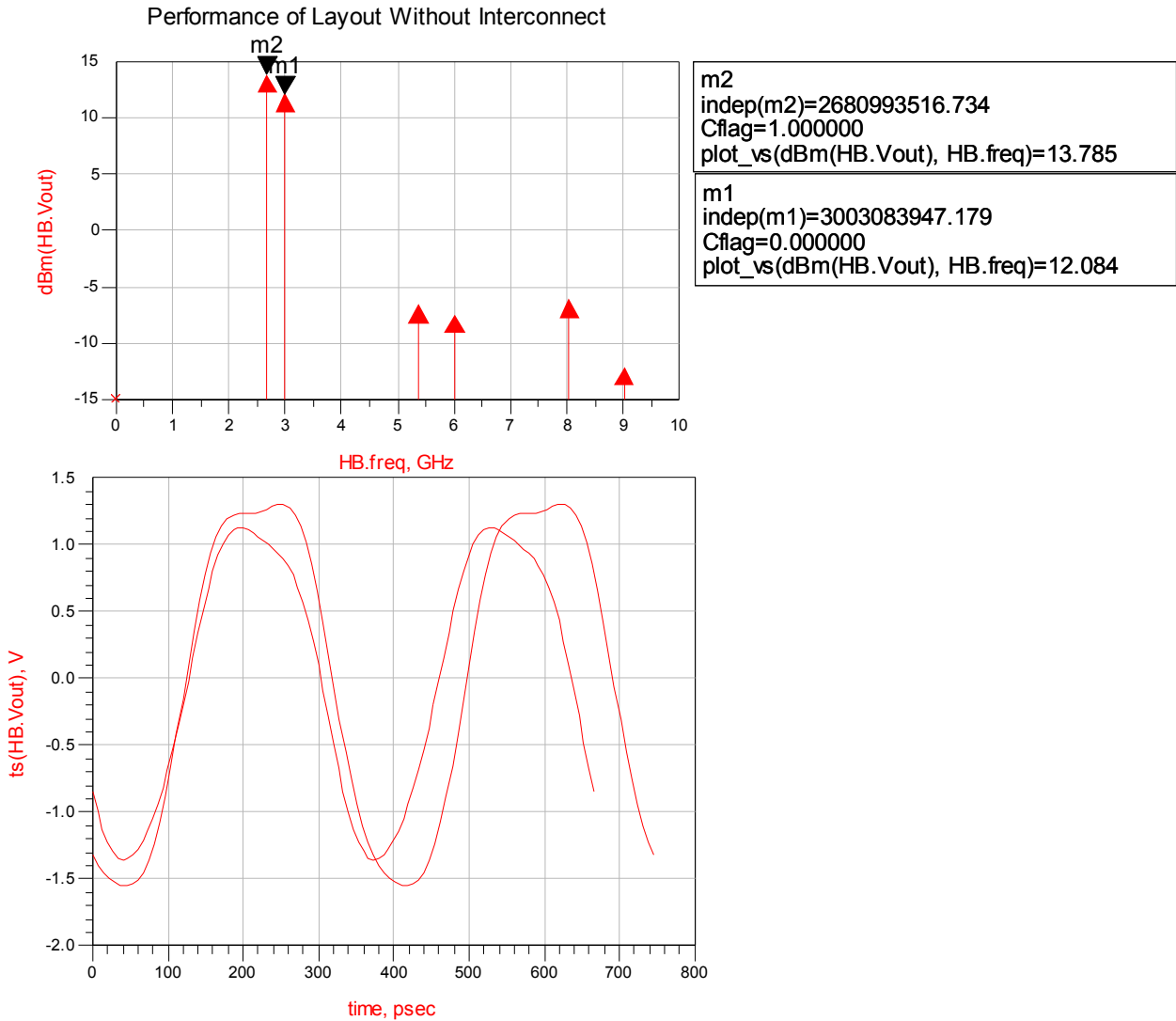
Another compromise was made for the output match versus the power output. A smaller output device could have been used to match 50Ω since it could have been sized such that $1/g_m$ equaled 50Ω , but the design is current limited in driving the output. More current was thus run in the source follower stage to drive the output and it was deliberately chosen to not match the output to minimize power loss and save area.

III. Modeled Performance Specification Matrix

VCO with on chip high Q resonator and tuning varactor.

<i>Specification Description</i>	<i>Specification</i>	<i>Design Performance</i>	<i>Compliance</i>
Frequency	2712 - 2813MHz	2596 - 2893 MHz	Specification Achieved
Output Power	>+ 5dBm	14.287 - 12.259 dBm	Specification Achieved
Output Power Goal	+10dBm	14.287 - 12.259 dBm	Goal Achieved
Control Voltage	0 – 5 Volts	0 – 5 Volts	Specification Achieved
Supply Voltage	+/- 5 Volts	+5V	Specification Achieved
Supply Voltage Goal	+5V	+5V	Goal Achieved
Output Impedance	50Ω (nominal)	50Ω (nominal)	Specification Achieved
Size	60 x 60 mil ANACHIP	60 x 60 mil ANACHIP	Specification Achieved

Figure 6. Specification Compliance Matrix.



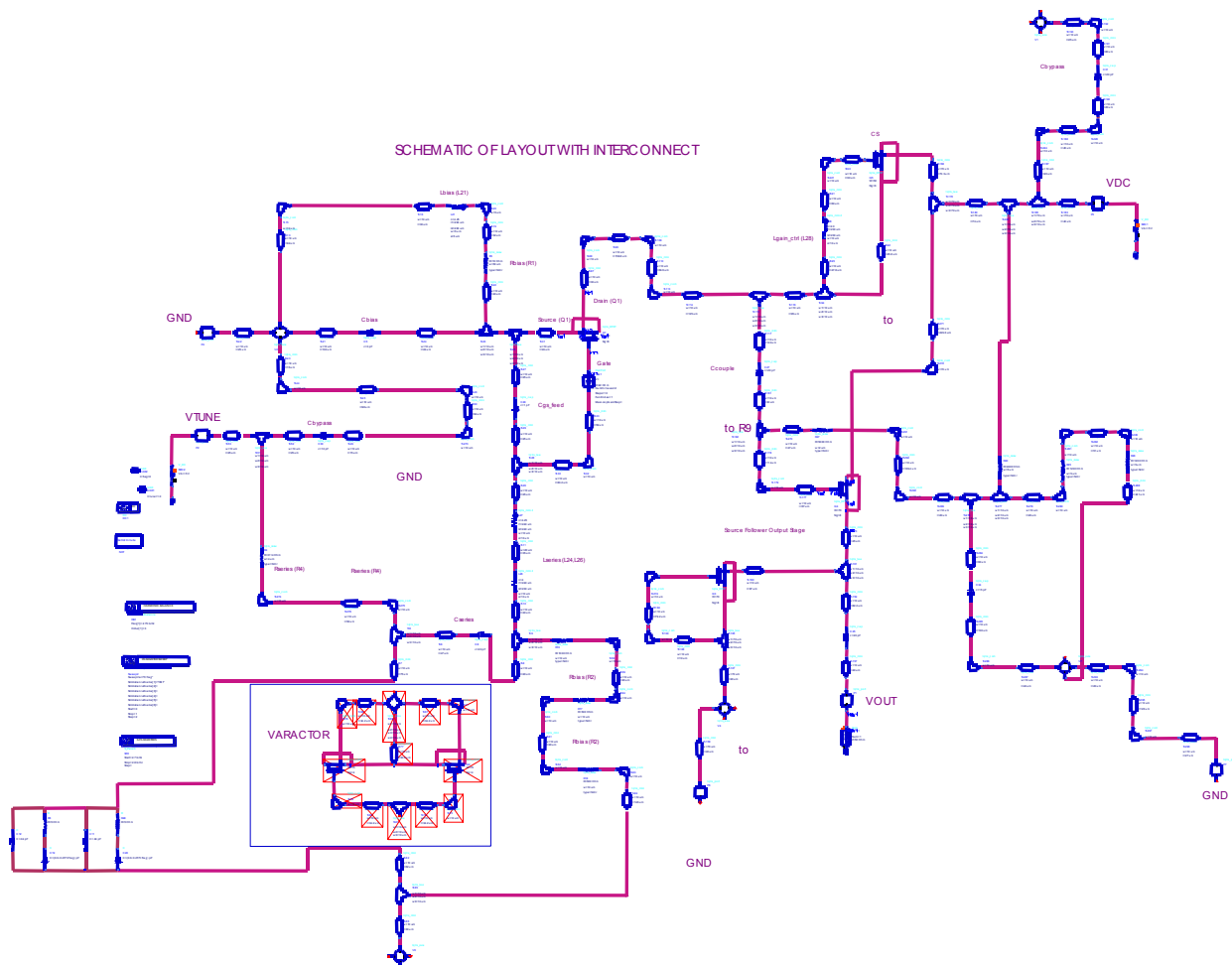


Figure 9. Post-Layout: VCO Schematic with Interconnect.

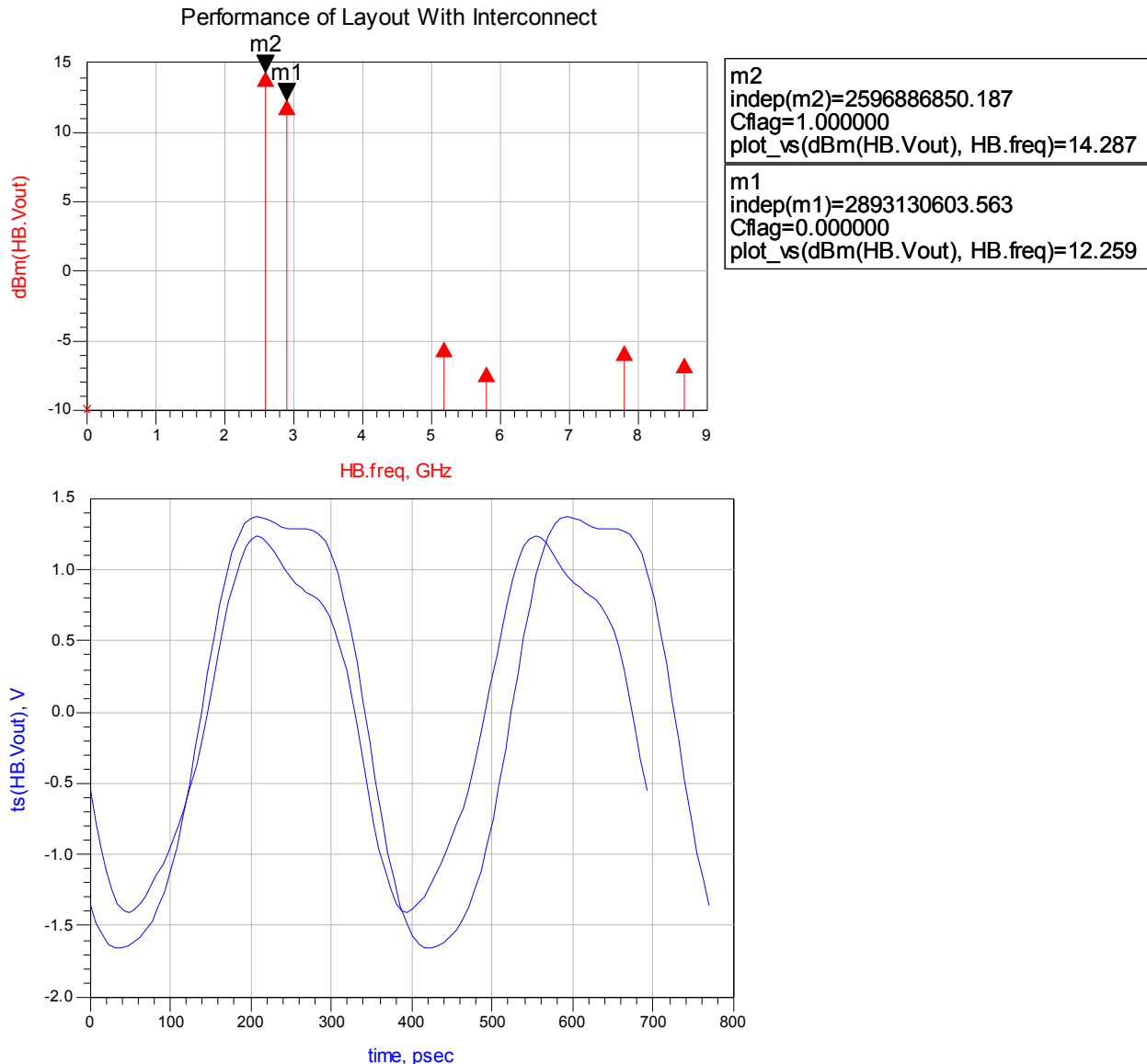


Figure 10. Post-Layout: VCO Performance with Interconnect.

When the results of an AC layout simulation with interconnect are examined as shown in Fig. 11, it can be seen that the VCO design satisfies both start-up conditions for steady state oscillation.

Marker M1 designates the real portion of the impedance looking into the resonant tank (Z_1 ; the load resistance), whereas marker M2 is the real portion of the impedance looking into the gate of the oscillator FET (Z_a ; the negative active resistance). Note that the absolute value of the negative active resistance is approximately twice the value of the load resistance which is less than the factor of three desired. This is an effective compromise between gain and signal compression and still essentially satisfies the start-up condition where $|R_a| \sim \geq 3R_1$.

The minimum oscillation frequency occurs when the minimum control voltage (Cflag = 1.000) is applied and observed at marker M3 equal to 2.512GHz when the corresponding line crosses the frequency axis equivalent to $Z_a + Z_1 = 0$. Conversely, when the maximum oscillation

frequency is applied (Cflag = 0.000), the maximum oscillation frequency is observed at M4 equal to 2.825 GHz. Note that the deviations in oscillation frequency as compared to previous simulation results are attributed to the differences in numerical solving methods between linear AC simulations and harmonic balance simulations.

Finally, observe that the top two unlabeled traces of Fig. 11 exhibit positive slopes for the imaginary portion of the impedance's looking into the resonant tank at both minimum and maximum control voltages (Cflag = 1.000, Cflag = 0.000) satisfying the condition where $[dX_1/d\omega]_{\omega_0} > 0$ is required.

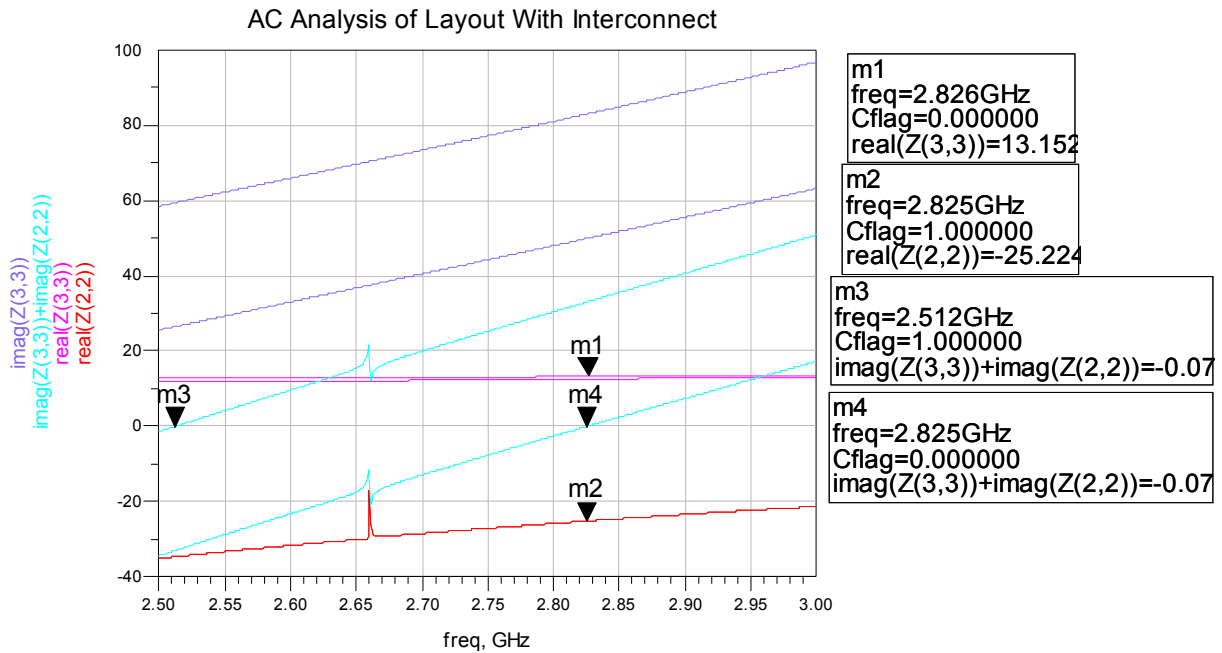


Figure 11. Post-Layout: AC Analysis of VCO with Interconnect.

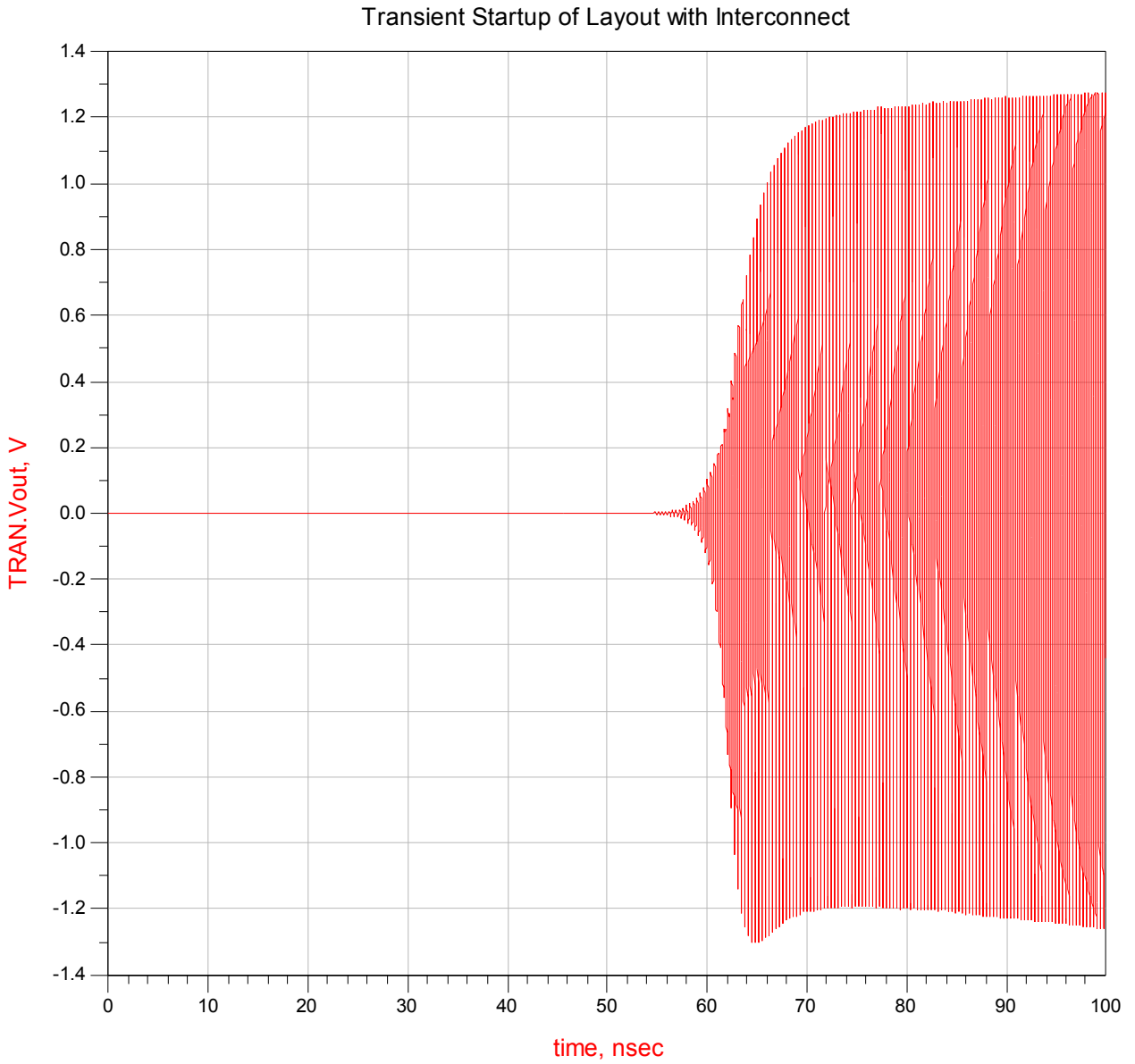


Figure 12. Post-Layout: Transient Analysis of VCO with Interconnect.

V. DC Analysis

A. Simplified DC Schematic

The original schematic without interconnect was edited such that all inductors were replaced with shorts and the capacitors opened, given that at DC, the frequency is zero. This is done to check for any inadvertent biasing shorts, shorting of the supplies, and to follow the biasing path.

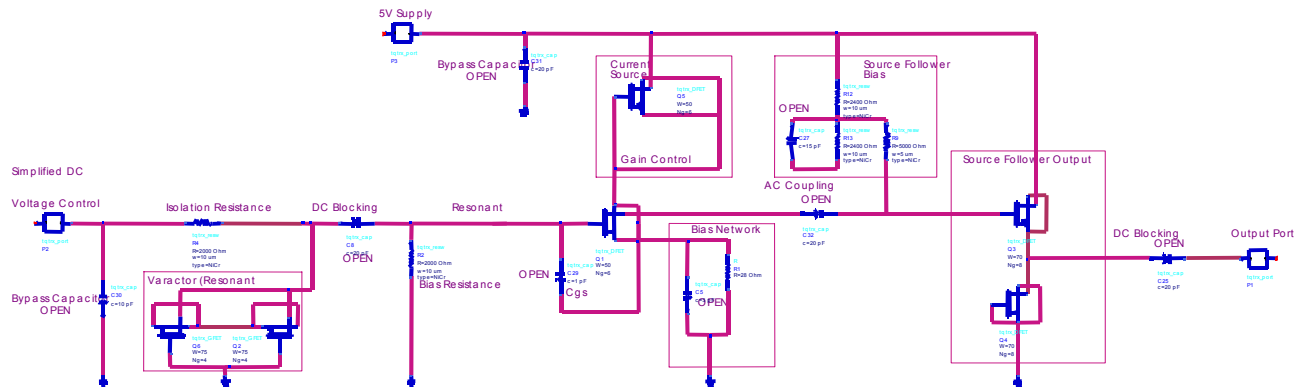


Figure 13. Simplified DC schematic of VCO.

B. Bias Check

<i>FET</i> (<i>tqtrx_DFET</i>)	<i>Function</i>	V_{GS} (mV)	V_{DS} (Volts)	I_{DS} (mA)
Q1	VCO FET	-203	4.5	12.8
Q5	VCO FET Current Source	0	0.290	12.8
Q4	Source Follower	0	2.5	40.9
Q3	Source Follower Current Source	0	2.5	40.9

Figure 14. DC Operating Points.

C. Interconnect and Component DC Current Stress

The VCO was simulated at DC and the current and voltage values at each of the circuit nodes were annotated upon the schematic. Based upon the TQTRx process design rules with respect to FET current handling, passive component current handling, and metal current density, no current thresholds appear to be violated.

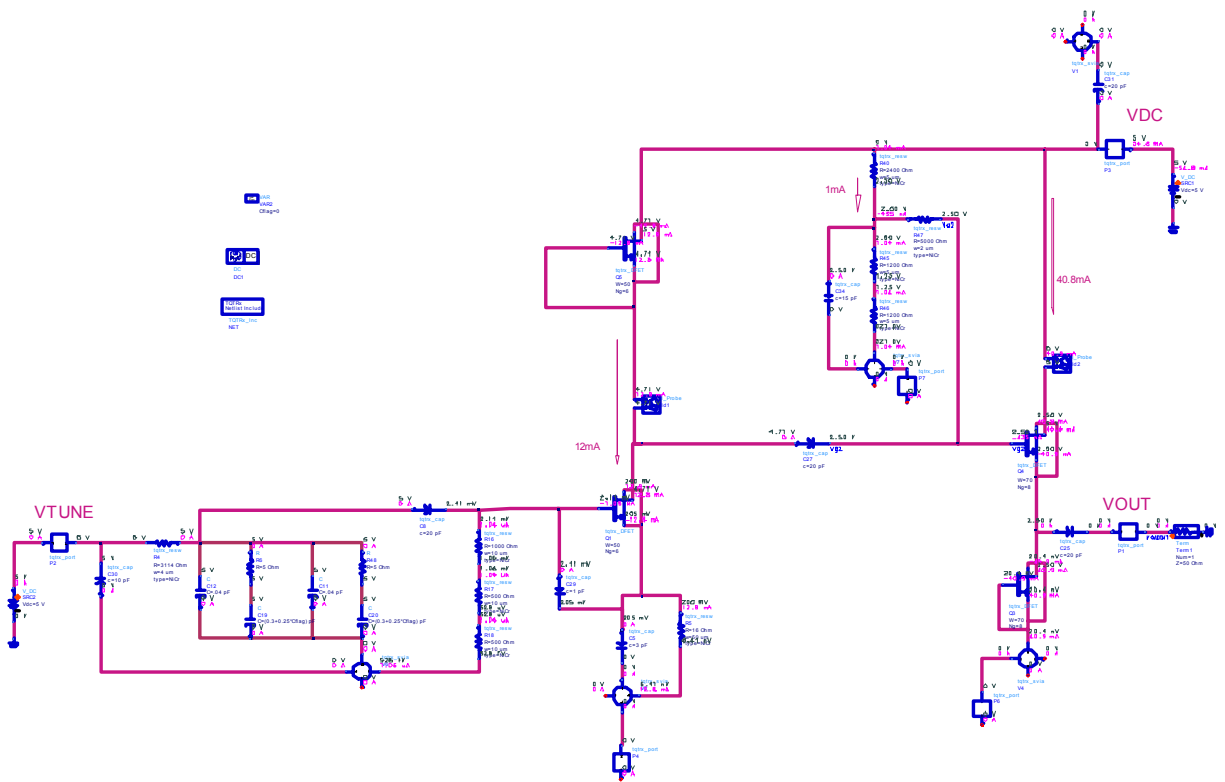


Figure 15. Interconnect and component DC current stress.

VI. Layout

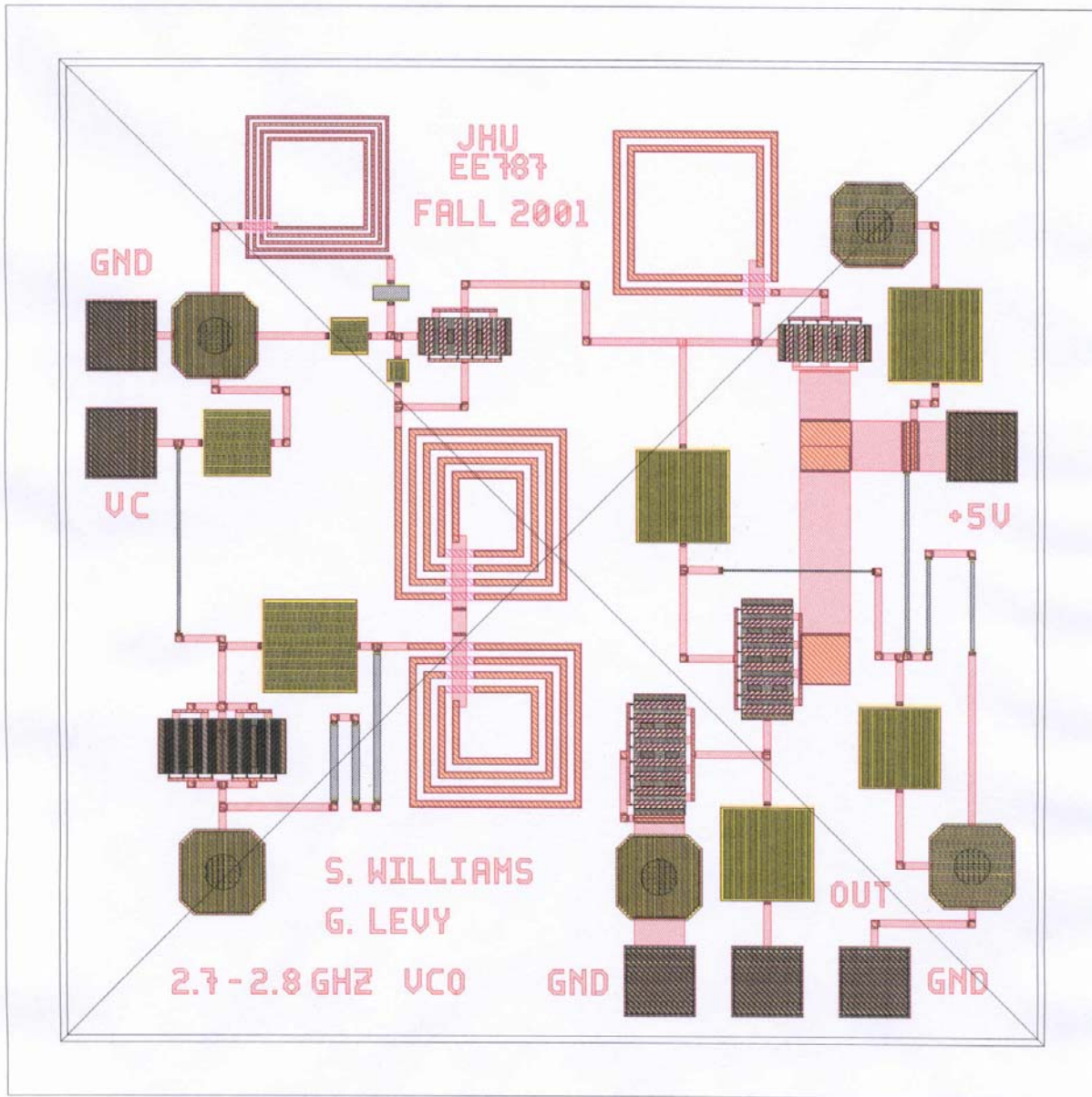


Figure 16. VCO layout.

VII. Test Plan

The bias (5 Volt supply) and frequency control (0-5 Volt variable supply) is applied to the designated pads on the layout with needle probes.

See Fig. 14 for the respective DC bias points for each transistor. Total DC current consumed by the VCO is ~55mA (the sum of each of the transistor bias currents at DC and the resistor ladder.)

The RF output should be extracted with ground-signal-ground (GSG) probes to a spectrum analyzer. The expected signal at the output should be a ~2 Volt peak to peak sinusoid, oscillating between 2596 MHz to 2893 MHz with corresponding power of 14.287 dBm to 12.259 dBm.

VIII. Conclusion & Recommendations

Given more time, a greater effort would have been spent to develop a more robust and innovative adaptive bias technique to limit the harmonic contribution to the output signal at the oscillation frequencies of interest while still maintaining a high gain at DC for startup.

Finally, given the design constraints for a HyperLan and or ISM frequency system, the VCO based upon schematic simulation results, layout simulation results, and peer and expert review, should both meet and or exceed each of the given VCO specifications.

IX. Acknowledgements

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