

2 Bit Phase Shifter

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Abstract

This report describes the design and simulated performance of a 2-Bit Phase Shifter which will be fabricated as a GaAs Monolithic Microwave Integrated Circuit (MMIC). This 2-Bit Phase Shifter is part of larger class project to implement a duplex transceiver for C-band HiperLAN wireless local area network for the industrial scientific and medical (ISM) frequencies. The design process was conducted with Microwave Office version 6.03 from Applied Wave Research using TriQuint semiconductor elements to fabricate capacitors, inductors, resistor, and FETs on a GaAs substrate.

Introduction - Phase Shifter

The 2-bit phase shifter is constructed as a two stage series phase shifter. The first stage switches between +45 and -45 degrees. The second stage switches between +90 and -90 degrees. There is a total swing of phase between -135 and +135 degrees in 4 steps of 45 degrees.

Each stage is controlled by a single control voltage or “bit” which applies complementary voltages to two pair of FET gates. When one voltage is “on” or 0 volts and the other is “off” or -5 volts. This process routes the RF signal through either a phase lead or phase lag network in each stage.

The design met the following specifications for 2 bits with control voltage of 0 /-5 volts. The return loss (S11) was less than -10dB.

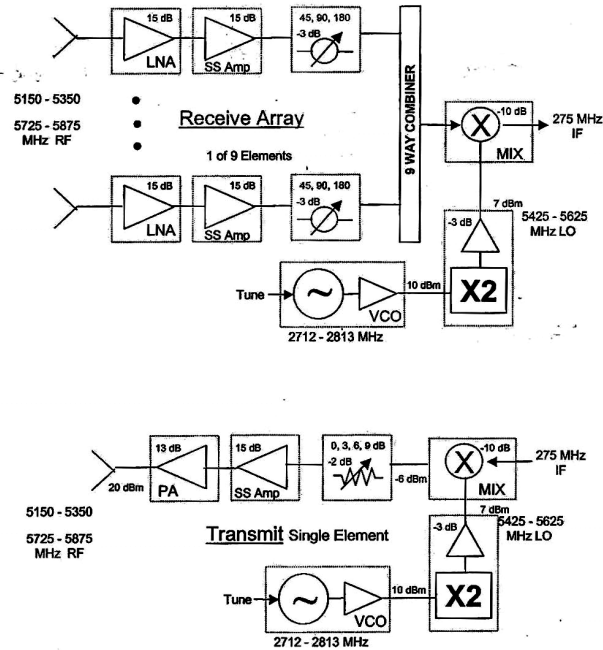
SPECIFICATIONS FOR 3 BIT PHASE SHIFTER

Goal: FET switches with on chip TTL driver

FREQUENCY:	5150 to 5875 MHz
BANDWIDTH:	> 800 MHz
INSERTION LOSS:	< 4 dB min IL (3 dB goal);
INSERTION BALANCE:	+/- 1dB min IL;
PHASE SHIFT:	steps 45 (goal), 90 and 180 degrees
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	± 5 Volts
CONTROL:	TTL (goal); or 0, -5V switch inputs
SIZE:	60 x 60 mil ANACHIP

The phase shifter is part of a duplex transceiver for C-band HiperLAN wireless local area network (WLAN) for the industrial scientific, and medical (ISM) frequencies.

The following is a block diagram of the class project:



Chip Set for the 5150 - 5350 MHz WLAN and
5725 - 5875 MHz ISM Bands

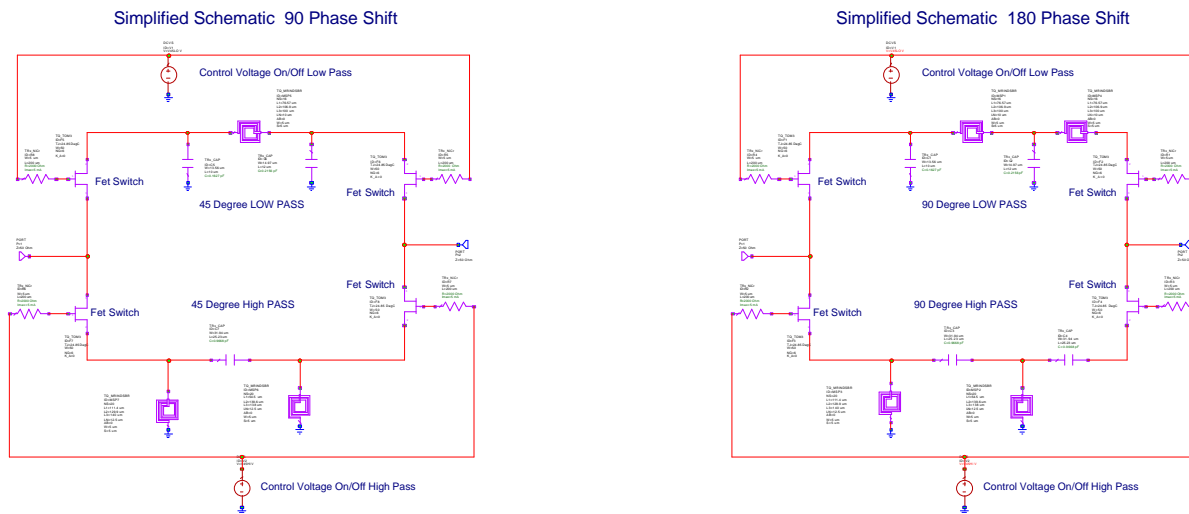
Design Approach

Before discussing the design approach, the following is a simplified schematic and a brief circuit description.

Each individual stage consists of 4 FET switches and two filters. The 2 top and 2 bottom pair of switches are toggled together. By applying complementary voltages of 0V and -5V to the top and bottom control voltages, respectively selects the top filter. Conversely applying -5V and 0V to the top and bottom controls, respectively will select the bottom filter.

The top filters of each stage are low pass filters and the bottom filters are high pass filters. The corner frequency of the low pass filters are set at approximately 1 GHz above the design frequency range (5.15GHz to 5.875GHz). The high pass filters corner frequency is set at approximately 1 GHz below the design frequency range. The high pass filters provide phase lead and the low pass filters provide phase lag.

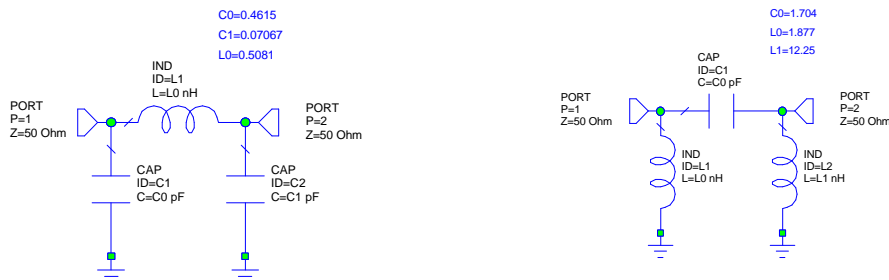
The following is a simplified block diagram of each stage:



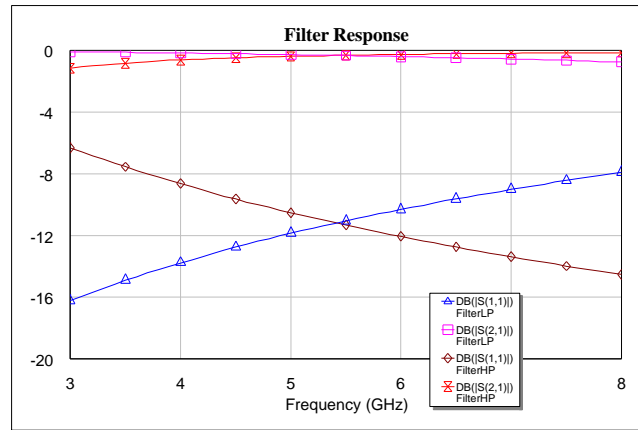
Selection of Topology

The first step is to settle on a topology for the low and high pass filters. A 3 pole filter using capacitors and inductors was selected for the 1st stage. A 4 pole filter topology was selected for the 2nd stage because of the need for greater phase shift. The critical concept here is that as more poles are added to each low pass filter or pole-zero pairs for high pass filter results in more phase shift. Balancing this requirement is the need to minimize insertion loss. Therefore as the corner frequencies are move closer and farther from the design band, the phase shift and insertion loss can be adjusted. The closer the corner frequency is to the design band, there is more phase shift and more insertion loss.

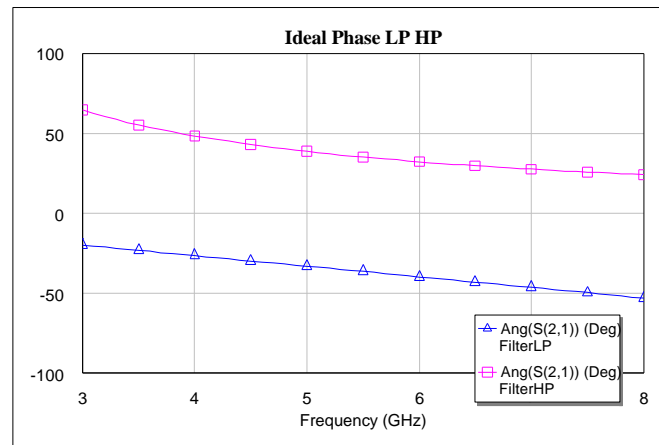
Using the filter wizard of MWO, the following initial component values of the low and high pass filters were selected.



The next graph shows the initial phase shift, insertion loss (S21) and return loss (S11) of the ideal low and high pass networks:



This is the first pass as the phase lead and phase lag of the 3 pole networks:



Trade Offs

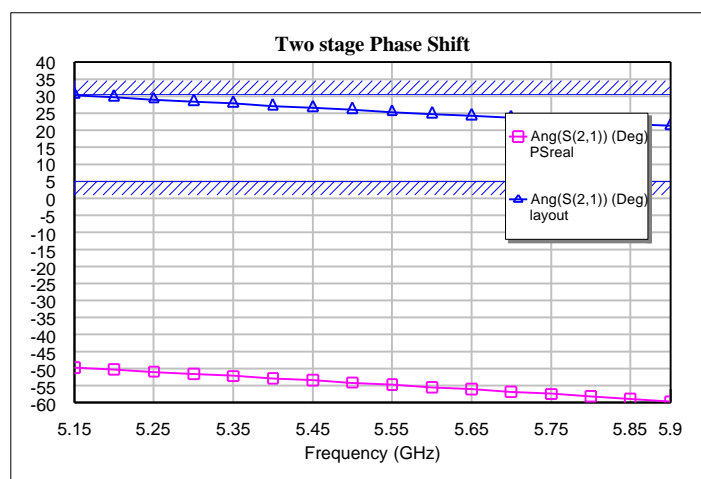
The next critical design decision is that 3 elements (and more) seems to work better because of the ability of compensating for the FET switches on either side of the filter. The FET switches can be modeled when they are “on” as a small series resistor and some small stray capacitance. The off FET switches can be modeled as a larger shunt capacitance. These capacitances can easily be compensated by the multi-stage filter. Also, the insertion loss is minimized when the filter looks like pi sections tuned to 50 ohms characteristic impedance. Another the way of visualizing this process is working with a Smith chart. The smaller capacitors and inductors are

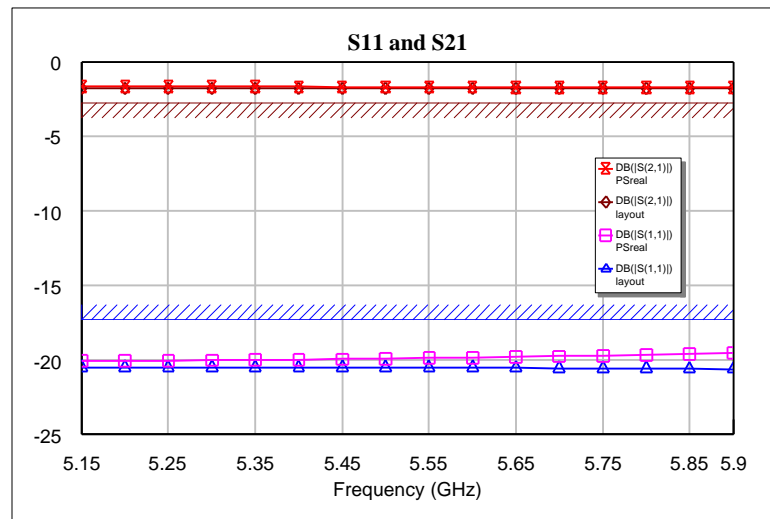
keeping the characteristic impedance closer to the origin (50 ohms) as opposed to a single large capacitor or inductor which moves the impedance farther away from the origin.

The obvious trade-off made during the design phase was to stick with just two bits. An attempt was made to use a one or two element phase shifter for +22.5 and -22.5 degrees. This would have been the third-bit or third stage of the phase shifter. There were design difficulties as discussed above using less than 3 elements. Also, at the time of the design phase it was unclear that a third stage would fit in the Anachip form factor. Also, a third stage would run very close to exceeding the 4dB insertion loss.

Optimization with MWO

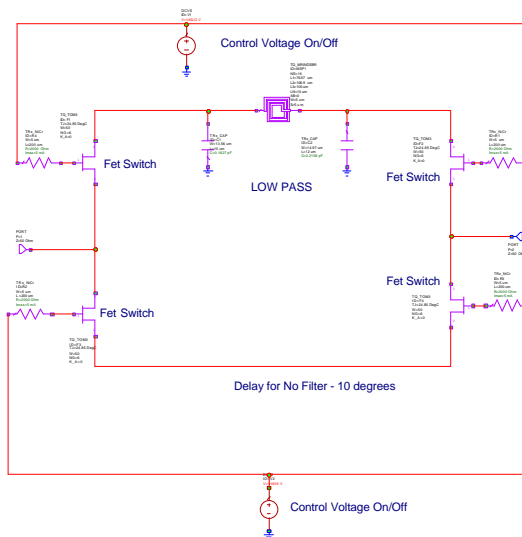
The following graphs show the design process after the initial selection of capacitors and inductors were made. The filters were inserted in the switching matrix and then the following constraints were imposed on the optimization wizard of MWO. The inductor and capacitor values were tightly constrained so they didn't drift too far. The insertion loss (S21) was constrained to be better than -3dB and the match (S11) was constrained to be less than -10dB. Then a second plot of phase was also constrained so the phase of the circuit could be adjusted up or down as needed. This process seemed to work quite well as long as the steps were small. Once the phase was adjusted to the correct value, then the S11 and S21 constraints could be more tightly adjusted to optimize the circuit further. The optimization process only took a minute for each adjustment. If the process took more than a minute then the process was stopped and the constraints loosened and optimization restarted.





Then was one additional design process. After some initial adjustment, the phase lead circuit component values were larger than the phase lag. The harder work of the high pass circuit translated into not only larger component values but more insertion loss and less match. This also means the knee of the filter is moving closer to the design frequency. The following circuit was simulated to get an idea the ‘natural’ phase lag of the circuit without any filter.

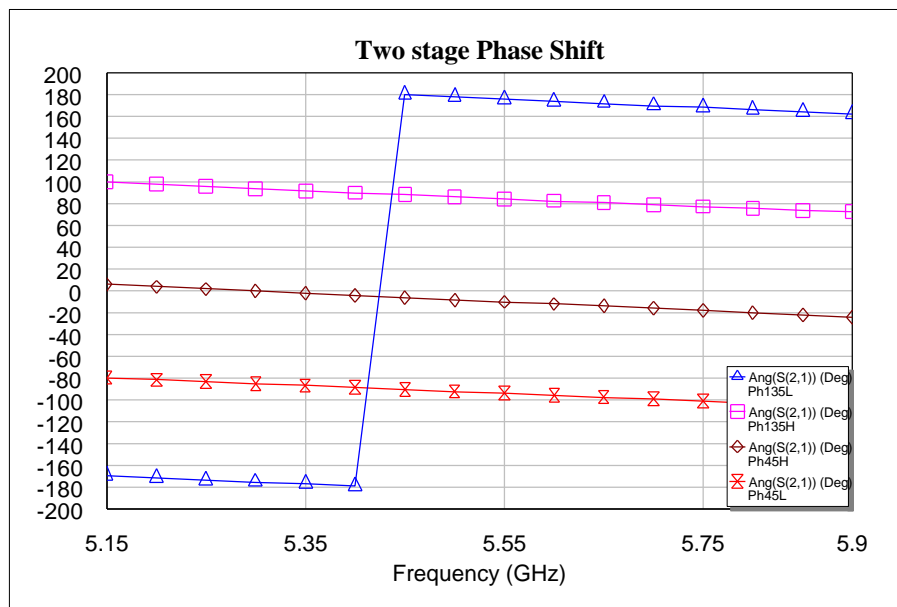
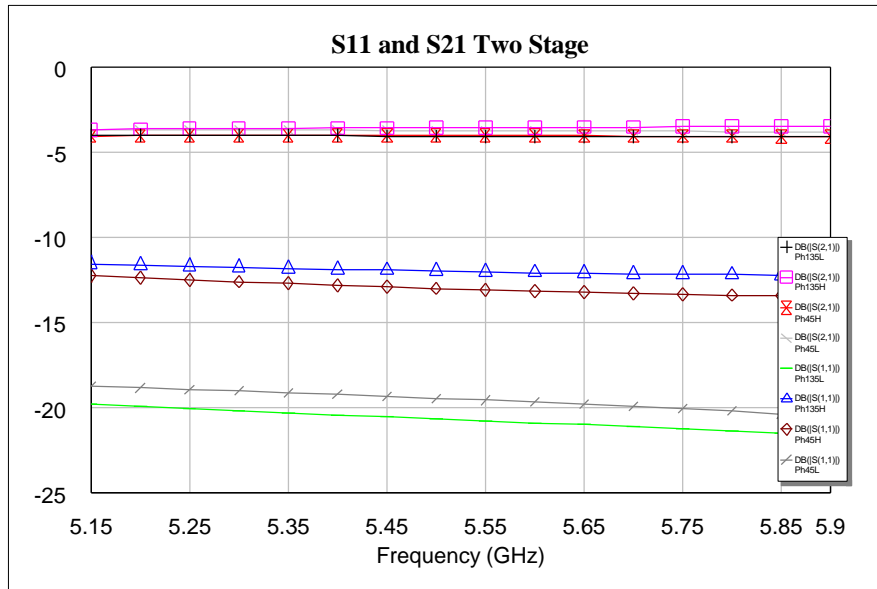
Simplified Schematic - Design Methodology



The lower path without any filtering had about 10 degrees phase shift. This offset put back into the optimization process so that the 45 degree phase lead circuit only needed to provide 35 degrees phase lead and the phase lag circuit needed to provide 55 degree phase lag. This balanced the circuits better in terms of sharing the insertion loss and match effects.

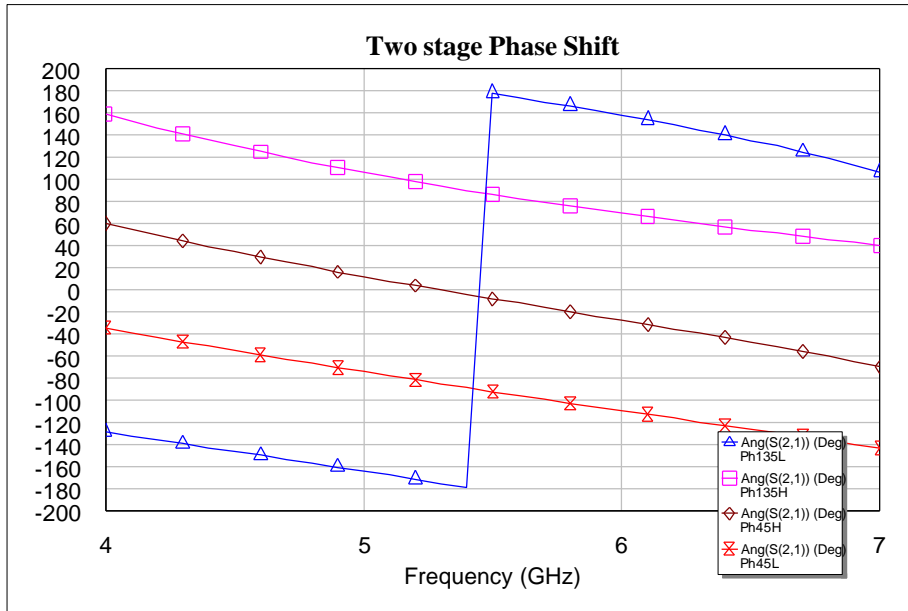
Simulations

The following is the circuit performance of the phase shifter showing the phase shift, insertion loss, and match over the design frequency:

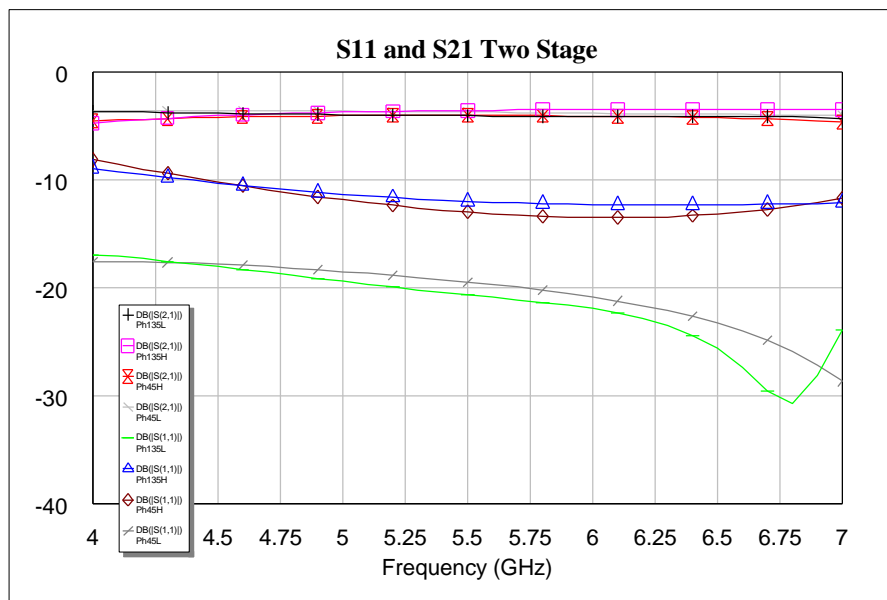


Note that the bottom blue line is the maximum phase lag, and that it folds back around after reaching -180 degrees.

These are the same plots but over a wider frequency range above and below the design frequency.

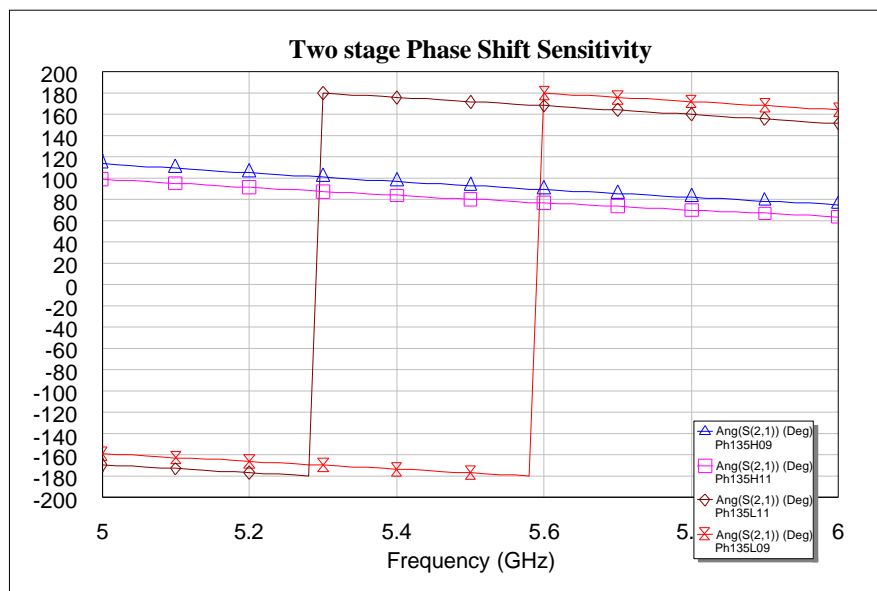
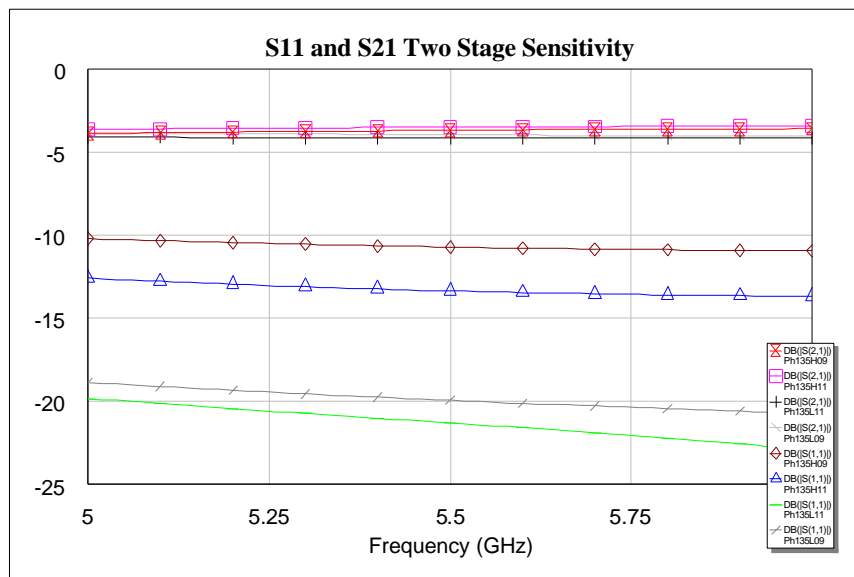


The insertion loss and match look reasonable outside the design frequency per the simulation.



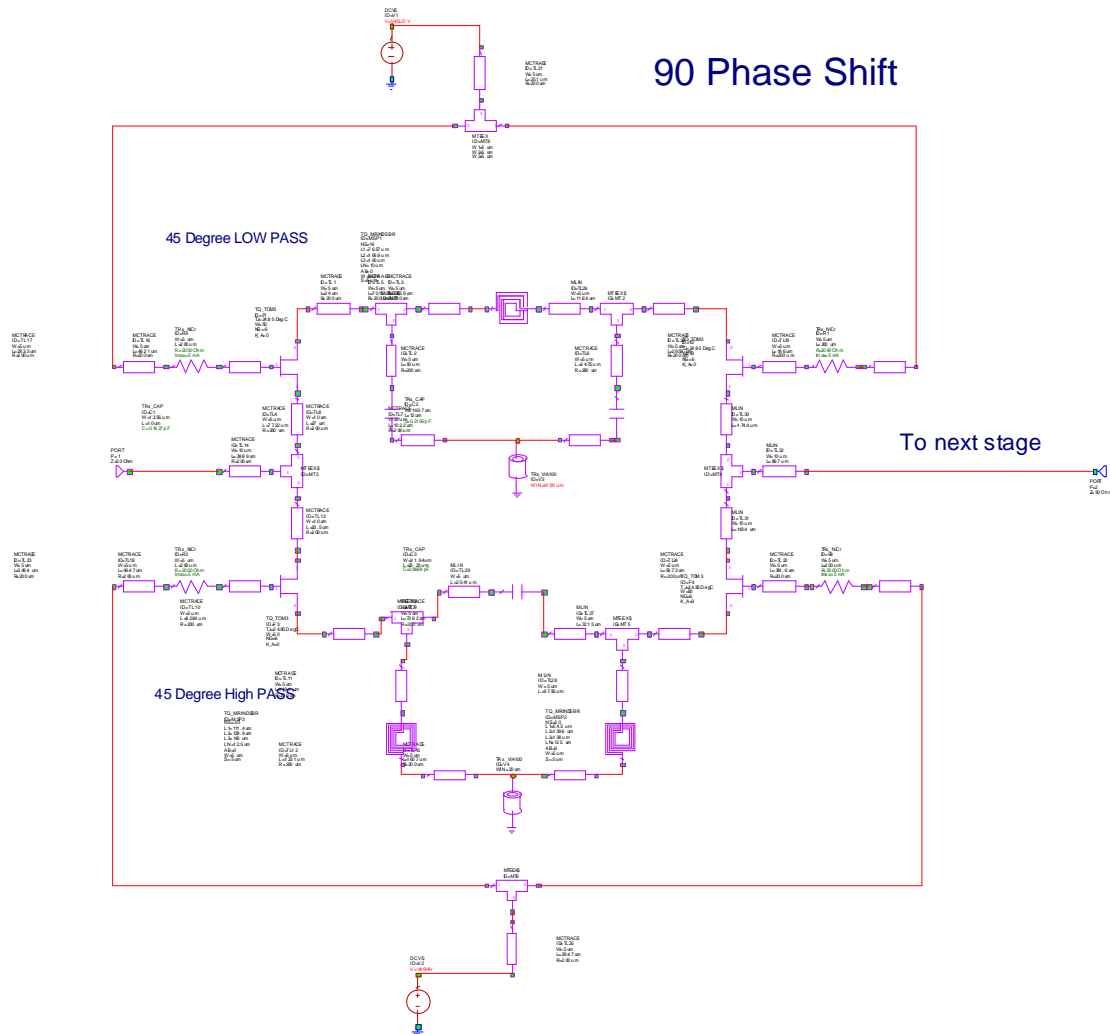
Sensitivity

The following plots attempt to characterize the sensitivity of the circuit to process variations. The inductor values should remain fairly constant but the capacitors will vary due to process variations with the thickness of the dielectric. Each plot below is for four schematics, two set at -135 degree phase shift and two at $+135$ degree phase shift. The capacitance of all the capacitors are varied $\pm 5\%$ around the nominal value for a total of 10% variation. From the phase graph, the sensitivity appears to be bounded at 2 degrees per 1% variation (i.e. less than 20 degrees for 10% variation). The insertion loss is less than 1 dB variation however the return loss (S11) varies by as much as 3 dB.

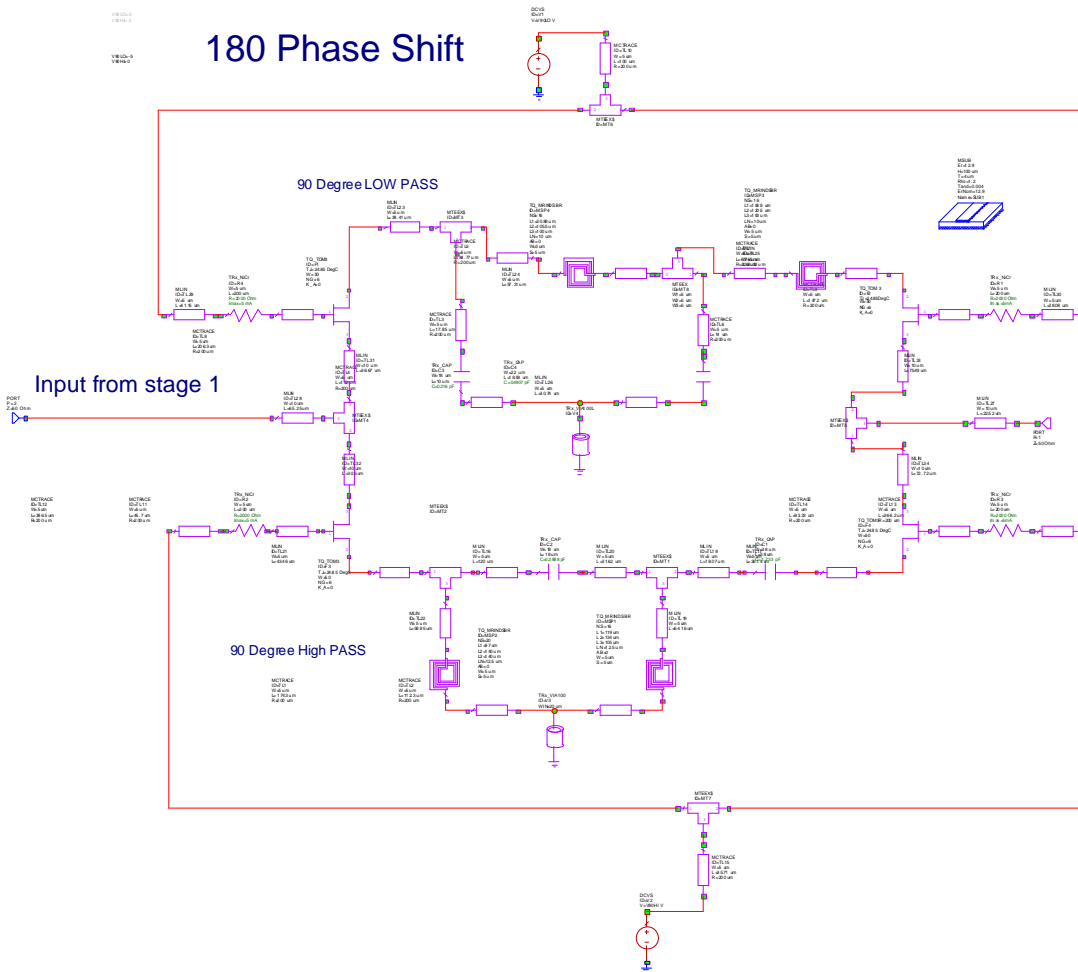


Schematic

The following is the completed circuit schematic including microstrip lines and TriQuint components for FETs, capacitors, inductors, resistors and ground vias. The Anachip pads for port connections and the additional ground pads and some ground vias are not shown in this schematic which are added to the layout. Also there are additional 2k resistors and ground pads attached to the sources of the switching FETs to provide a DC reference ground.

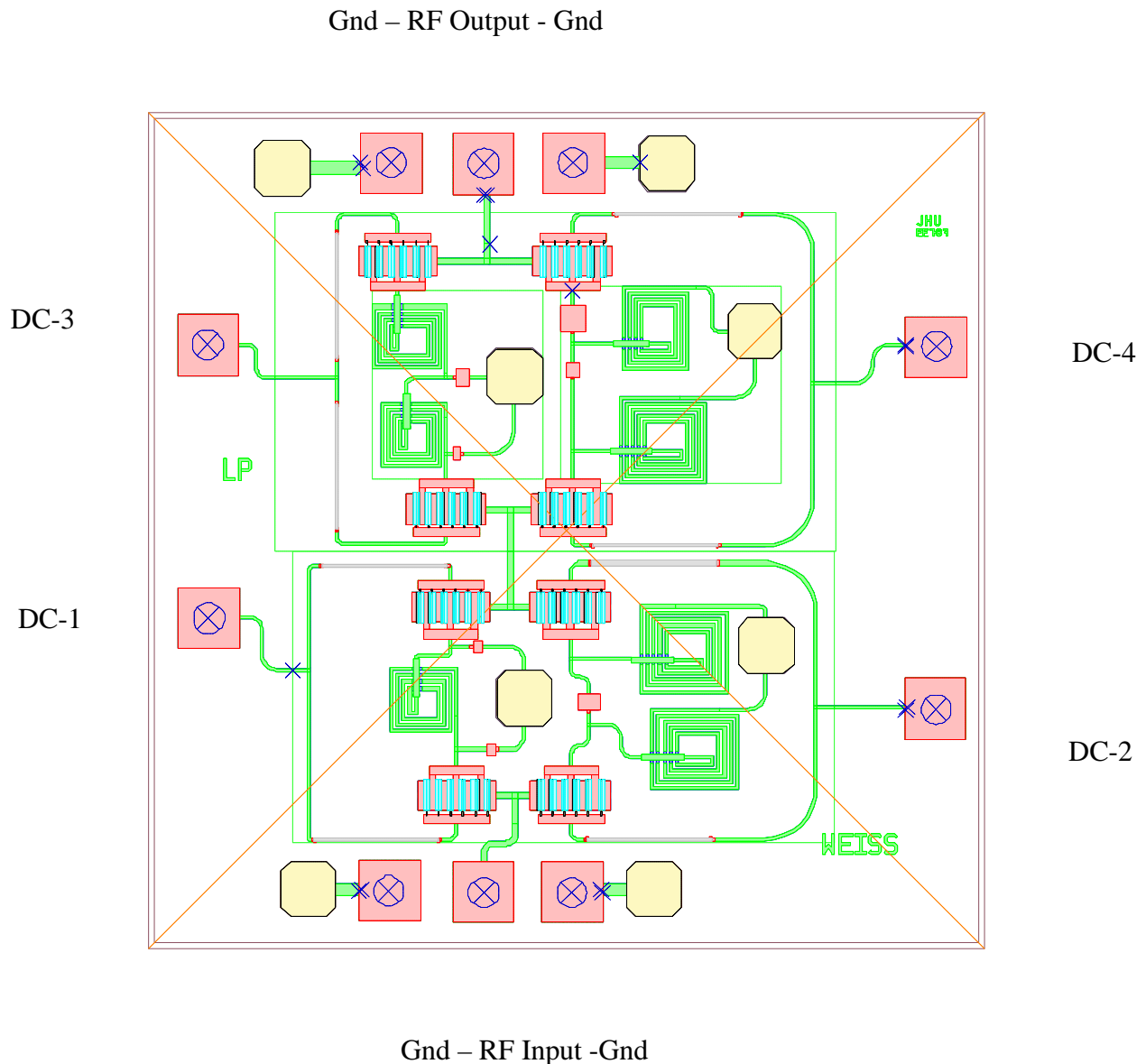


This is stage two with a 90 degree phase lead and a 90 phase lag network selected with the dual pair of FET switches.



Layout Plot

The input port is located at the bottom of the chip, the output port is at the top middle pad. There are ground-signal-ground pad configurations at each of these ports to facilitate probing. The lower left side control voltage pad controls the low pass network for the 45 degree phase lag circuit. The lower right control pad controls the 45degree phase lead circuit. Similarly the top left and top right control pads are for the 90 degree phase lag and lead circuits respectively.



DC-1 and DC-2 are complementary control voltage ports for stage 1. DC-3 and DC-4 are complementary control voltage ports for stage2.

Test Plan

Verification of the phase shifter will be with a network analyzer to measure the phase shift for each of the four states of phase shift: -135, -45, +45, +135.

Equipment:

Network Analyzer 8510

Probing Station

Power supply to provide 0V and -5V control voltages

Procedure:

- 1) Connect port1 of the Network Analyzer via the probing station to the input port with a ground-signal-ground configuration.
- 2) Connect port2 of the Network Analyzer via the probing station to the output port with a ground-signal-ground configuration.
- 3) Connect -5V via the probing station to: DC-1 and DC-3 control voltage ports
- 4) Connect 0V via the probing station to: DC-2 and DC-4 control voltage ports.
- 5) Perform a sweep from 3 GHz to 7GHz on the Network Analyzer . Save the results of the s2p file to disk. The sweep will have magnitude and phase information of all the S parameters: s11 ,s12, s21,s2.
- 6) Connect -5V via the probing station to: DC-1 and DC-4 control voltage ports
- 7) Connect 0V via the probing station to: DC-2 and DC-3 control voltage ports.
- 8) Perform a sweep from 3 GHz to 7GHz on the Network Analyzer . Save the results of the s2p file to disk.
- 9) Connect -5V via the probing station to: DC-2 and DC-4 control voltage ports
- 10) Connect 0V via the probing station to: DC-1 and DC-3 control voltage ports.
- 11) Perform a sweep from 3 GHz to 7GHz on the Network Analyzer . Save the results of the s2p file to disk.
- 12) Connect -5V via the probing station to: DC-2 and DC-3 control voltage ports
- 13) Connect 0V via the probing station to: DC-1 and DC-4 control voltage ports.
- 14) Perform a sweep from 3 GHz to 7GHz on the Network Analyzer . Save the results of the s2p file to disk.
- 15) Compare actual results with simulation results for magnitude of S11, S21, S22 and phase of S21.

Summary & Conclusions

Most of the design criteria were met for the 2-bit phase shifter. The insertion loss was better than the 4dB specified and the VSWR goal of 1.5:1 ($S_{11} < -14\text{dB}$) was approached with S_{11} better than -11dB (VSWR 1.8:1). The insertion balance was within the 1 dB specified across the frequency band. With the experience of this design, it might be possible to fit the third bit phase shifter which would shift between -22.5 and 22.5 degrees.

Although not the first time that MWO was used as a Cad tool, it performed reasonably well. The simulations were completed with reasonable ease. However with the layout tool, there were some connection problems that produced a warning message even though the connections were made. The newer version of software 6.5 fixes this problem with more robust connection surfaces using a "variable" setting on the faces. If a component is slightly off-grid the 6.03 software registered an error when two connection faces were "connected".

The more significant issue is the fabrication and verification of the design using MWO. A successful track record has been established with another CAD tool and so it remains an issue to see how well the designs with MWO prove out under scrutiny of a probing station applied to the MMIC die.